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HIGH-LEVEL STRUCTURAL TEST PARALLELISM

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Abstract

Tests used traditionally to have been developed by the systems company based solely on knowledge of the components' functions, obtained from product documentation. This process has become considerably more difficult as the complexity of the components has increased, leading to a rapid escalation in test development costs. This required an earlier high-level test development optimization and minimization. Techniques employed in this high-level test methodology are surveyed in this paper.

1 INTRODUCTION

Test development time required for VLSI components can range from several weeks, in the case of non-difficult single chips, to a few years, in the case of big MCMs [Fli94]. The test development time depends on chip complexity, required fault coverage, and the ability to perform accurate simulation. When the test is already developed, the *production test* and *field test* could suffer from *test application time* and *power dissipation* points of view, unless they have been optimized during test development. Thus, even though the production chip testers are available with test speeds higher than 100 million patterns per second, and the typical tester memories are bigger than 1 million patterns, the complexity and the dimensions of nowadays electronic systems (e.g. MCMs) determine the need for additional *test application time optimization with power dissipation constraints.*

2 MULTI-CHIP MODULE AND ITS TEST

Products motivated by performance-driven and/or density-driven goals have started to use huge VLSI designs as the MCM technology, even though this technology still has several challenging problems, that need to be resolved before it comes a widely adopted solution. Since more than 35% (up to 60%) of MCM building cost is for its testing and diagnosis, one of the most challenging problem in this context is achieving acceptable MCM product quality requirements [CCBC98]. This can be significantly reduced by adopting adequate testing approaches which: guarantee the quality of incoming bare (unpackaged) dies prior to module assembly, ensure the structural integrity and performance of the assembled MCMs, and help isolating defective parts prior to the repair process.

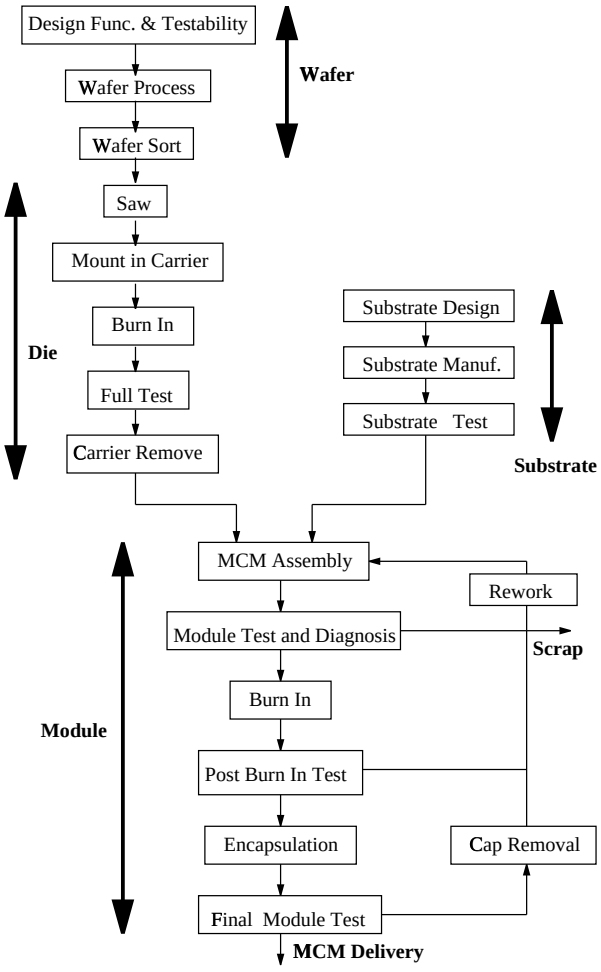


Figure 1: MCM Production and Test Flow

MCM testing is depicted in figure 1. It is consisted of the following four stages [Zor94, Zor97a]: wafer test, bare die test, substrate test, and MCM assembled test and repair. During *wafer test*, chip suppliers traditionally perform a simple wafer test, which consists of running: functional test - a structural integrity test at low speeds, input/output parametric test - checks if finished wafer/dies meet input/ouput voltage and leakage specifications.

The *bare die test* should normally be carried out after the chip was packaged. However, in the MCM technology, bare dies are not packaged anymore because they have to be attached directly to the substrate. The bare die test consists of a comprehensive performance and reliability test, and implies the following test steps. Firstly, a *parametric test*, which is similar to the one performed in the wafer test, where it is verified that finished dies meet input/output voltage and leakage specifications. Secondly, a *functional at-speed test*, which is a comprehensive performance test most probably employing built-in self-test (BIST) design methodology usually through boundary scan (BS) instructions. It can be seen as a performance test needed to detect delay type faults which are not manifested during the conventional low speed wafer level test [SLAL94]. Thirdly, a *reliability test* step is employed to perform professional stress testing in order to ensure the highest IC quality.

The *substrate test* stage is meant to test MCM substrates for electrical integrity (open and short failures) prior to attaching the bare dies. Finally, *MCM assembled test and repair* has to ensure that all dies are properly connected, that they are still functionally correct and that the MCM as a device meets its performance specifications.

Having the test steps for an MCM, the typical defects that are usually generated during the assembling of the dies on the substrate at MCM level could be defined. *Trace opens* generally occur due to faulty attachment of the die (or encapsulated die) to the substrate. *Trace shorts* will also typically result from a faulty attachment of the die (or encapsulated die) to the substrate. Typical shorts are due to solder bridges between pads, cross bonding of a wirebond, etc. *Improper device orientation* emerge frequently when dice, which are symmetrical, are mistakenly inserted into a circuit in two or more orientations. *Damaged die* that might be caused by the handling of unpackaged or encapsulated dice and results in electrical or mechanical damage to the device. *Wrong component* assumes the insertion of an improper component since many dice look alike and are typically not marked.

3 MCM TESTING AND THE BOARD TEST APPROACH

In MCM or PCB design, it is often useful, for purposes of testing and fault isolation, to be able to isolate one module from the others. This can be done using the concept of boundary scan (BS), which is illustrated in figure 2. BS support consists of an instruction register, a data register, scan cells, and associated logic, all of which are accessed through the test access port (TAP). The TAP interface consists of three inputs - TMS, TDI, and TCK - and one output, TDO. It can be noticed in this figure that BS cells are inserted between IC's internal logic structure and IC's pins themselves. The BS path is designed by chaining all BS cells. These BS cells are transparent in the normal mode. That is, normal inputs are connected to the internal logic's inputs. BS cells are activated in the testing mode when this BS chain can be loaded or unloaded by shifting in preloaded values or, respectively, shifting out sampled values. This system is very efficient for testing inter-chip connections and in-chip hardware. The initial reasons for using BS were to allow for efficient testing of board interconnect and to facilitate isolation and testing of chips either via the test bus or by BIST hardware. However, the same technique can be used to test MCM structures.

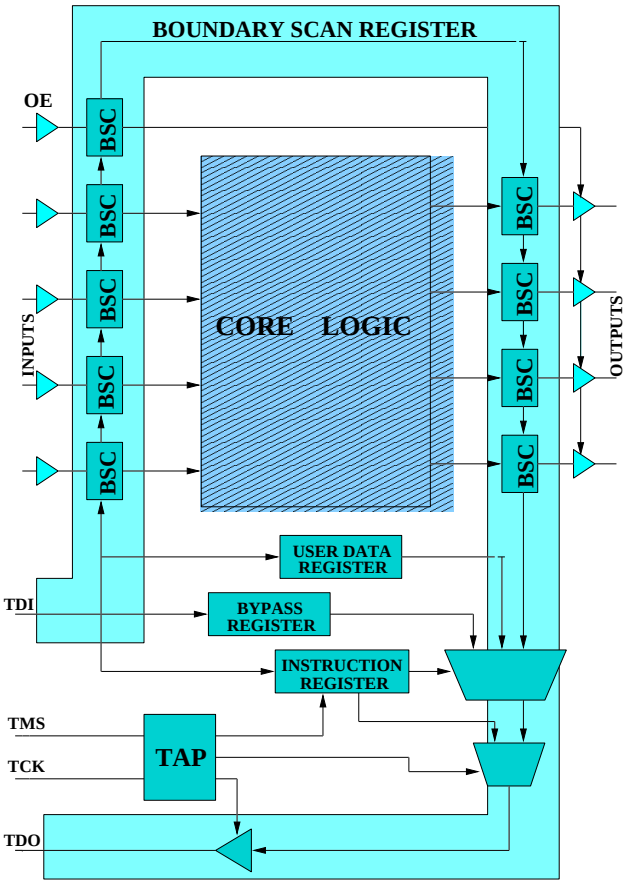


Figure 2: IEEE 1149.1 - JTAG Standard

On the other hand, the approach to treat the MCM also as a board requires that internal details be made visible to the user and that MCM design data be available. Thus, the main problem with MCMs is their dual personalities, that they need to be treated as boards by the manufacturer and that they must appear as devices to users in order to generalize the hierarchical view of the electronic systems.

The IEEE 1149.1a defines a "compliance enable mode" for an 1149.1 compliant device. This mode recognizes that at different stages in a device's life cycle (based, for example, on the level of integration hierarchy of the product) different test methodologies and protocols may be appropriate. The compliance enable feature permits a device to dedicate one or more (ideally few) pins for the purpose of enabling compliance. [Jar97] proposes an application of the compliance enable option to solve the MCM problem. Here, the MCM would have a BS compliance enable pin (BCE) and on this pin the MCM would be placed in either of the following two test modes: the *STAND-alone* test mode, in which case the MCM would appear as a small board. This is actually the mode in which a MCM manufacturers would test the MCM. The *embedded* test mode, where the MCM would appear as a fully 1149.1 compliant device. This mode would be used by a user to test the MCM assembled on a board, as part of other BS devices.

4 BIST-BASED METHODOLOGIES FOR MCM TESTING

The design for testability (DFT) implementation of an MCM must begin at the conceptual stages in order for the benefits to be achieved. Firstly, at high-level, functional partitioning and allocation of MCM system requirements will establish the MCM operating environment, performance, size, power, and test requirements. Then, having the test methodologies selected for the different modules, and moreover for different blocks of the modules, an important task is to schedule the test application for a minimum overall test time, taking into account the power dissipation constraints. Once the conceptual design and test requirements have been defined, a test and diagnostic strategy is developed. A trade-off analysis of life cycle costs, design impact, and the benefits of the proposed DFT strategy is performed. This activity results in definition of the necessary DFT requirements for MCM design.

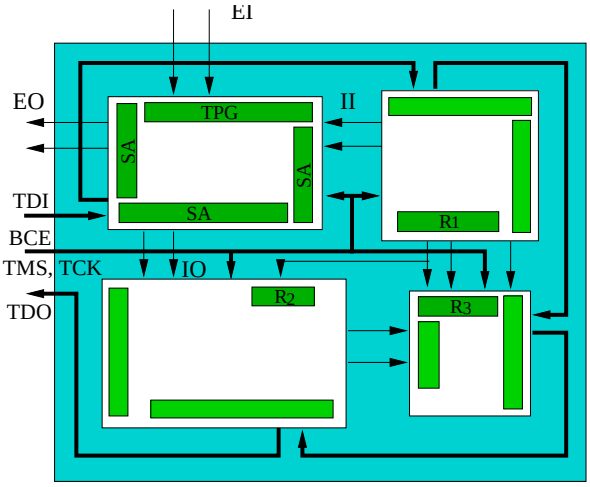
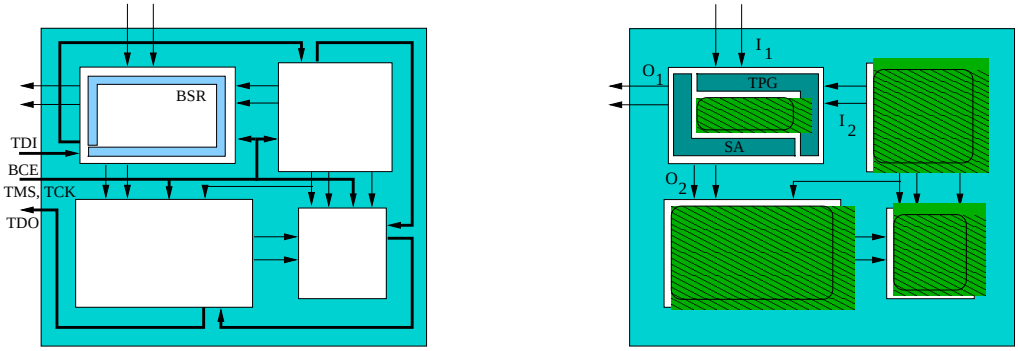


Figure 3: MC-BIST Architecture Example

MCMs are often used for applications requiring high performance and there are many factors that can contribute to an MCM not running at its expected speed. Examples of such factors, that reduce the performance of an MCM, are timing skews between chips, ground bounces, crosstalk between lines, variations in loading on the die outputs, and errors in the assembly process. It is for this reason that a performance test of the entire MCM at its system speed is necessary. BIST is a design technique in which parts of a circuit are used to test the circuit itself and it can be run also at full speed. Unfortunately, beside its best known efficiency and results, an area and delay overhead is added to the design. Moreover, the conventional single-chip BIST (SCBIST), used so far at device level, and BS do not provide performance test for the entire MCM. Multi-chip BIST (MCBIST) assumes that SCBIST is implemented in the random logic and the embedded cores. SCBIST is typically composed of: a full or partial chaining of flip-flops for pseudo-random testing in the random logic, while bypassing the individual embedded cores and their own BIST blocks [ZB97]. The MCBIST approach proposed in [ZB97] is based on structural testing, hence does not require knowledge about MCM's functionality. It is based on pseudo-random testing (LFSR based) and signature analysis (MISR based), which are reconfigurable to two structures: the first provides a SCBIST configuration, while in the second the LFSRs and MISRs are reconfigured such that the entire MCM operates as a single module with BIST, i.e. MCBIST (see figure 3). The solution given in [ZB97] augments the conventional SCBIST approach, which is used to produce individual good dies, to an effective MCBIST solution. The hardware design of multi-chip and single-chip self-test blocks is combined under one common architecture called the *Dual BIST Architecture*, an MCM testing employs: a full (static and dynamic) test for each mounted chip, a static test and diagnosis for interconnects, and performance test and diagnosis for the assembled MCM.

The SCBIST strategy, given in figure 4(a), emphasizes on having BIST and BS in the MCM chips [ZB97]. The creation of SCBIST-based ICs requires three major steps [Zor94]. The first

stage is the *planning stage* which consists of partitioning the chip based on *divide and conquer* approach to structural blocks like in figure 4(b). This approach is efficient from turnaround time point of view since all the optimization algorithms applied at this design stage can be conceived on divide-and-conquer basis, thus achieving near-optimal or even optimal solutions in a reasonable period of time. Following the partitioning, the schedule for BIST execution is planned, according to the specifications of the partitioned blocks, such as the number of identical blocks, their clock domain distributions, the floorplanning, and the BIST power dissipation of the partitioned blocks. The BIST planning is completed by identifying the BIST scheduling profile.



(a) MCM Example with Single Chip Test (b) MCM Example with Bare Die BIST

Figure 4: MCM Example with Boundary Scan and BIST Test Methodology

The second stage in the process is the BIST incorporation, which is basically the *hardware modification stage*. This starts with adopting an appropriate BIST scheme for each block type (e.g. a chip consists of random logic blocks, and regular structure ones). Depending on the performance considerations, area overhead limitations, and fault coverage requirements, a BIST schemed is selected for each block. The last stage includes the recombination of all BISTed blocks, the addition of the BIST control network, and the insertion of BS facilities.

Unfortunately, the use of conventional approaches (e.g. SCBIST test) to test the performance of MCMs faces three major limitations [ZB97]. The first limitation is the difficulty of writing or generating module level test patterns by conventional techniques. For small and simple MCMs, the development of patterns for performance test can be done by MCM designers. However, for the complex ones, it is almost impossible to generate test sets by using MCM level simulation. The second is the speed limitation of the tester. An MCM performance test requires a tester with the capability of high speed test vector application over high pin counts, which are nowadays very expensive if at all possible. The third is the problem of obtaining diagnostic information to locate the failed part. Module level probing techniques can provide such diagnostic information, but due to the density of today's MCMs probing turns out to be almost impossible.

5 CONCLUSIONS

The MCM design and test emphasized that the composing chips should provide a certain level of built-in testability. Even though lately most of the chips (die) are designed featuring

these built-in capabilities some of them still lack them. Thus the following solutions have been proposed to solve the low testability of the components without any DFT provisions. *Addition of BIST capability* to test some chips without BIST facilities in their design by adding a dedicated chip with BIST to test them in the MCM design. This is common for off-the-shelf memories where an ASIC circuit with BIST capabilities, based on regular structure schemes, is meant to provide self-testing of the memory arrays. *Addition of BS capability* around the chips without BS. In order to provide them with interconnect testing, the interconnects between the chip without BS and the chips around it having BS are tested by implementing a low complexity algorithm in the latter ones to be applied on the pins of the former one by means of their BS. In order to reduce the external logic required to test the MCM logic and to provide the MCM with a built-in test control capability (device for further system design and test use), a *Boundary Scan Master chip* can become a very effective component of an MCM to make it a self-testable device and perform the effective test operations by an autonomous manner. This autonomous test can be reused at all levels of test beyond module testing, i.e. board, system, field.

References

[CCBC98] S. Chattopadhyay, D.R. Chowdhury, S. Bhattacharjee, and P.P. Chaudhuri. Cellular-Automata-Array-Based Diagnosis of Board Level Faults. *IEEE Transactions on Computers*, 47(8):817–827, Aug 1998.

[Fli94] A. Flint. Test Strategies for a Family of Complex MCMs. In *Proceedings of The IEEE International Test Conference, ITC'94*, pages 436–445, 1994.

[Jar97] N. Jarwala. Designing "Dual Personality" IEEE 1149.1 Compliant Multi-Chip Modules. *Journal of Electronic Testing: Theory and Applications*, 10:77–86, 1997.

[Mir97] J.E. Miranda. A BIST and Boundary-Scan Economics Framework. *IEEE Design & Test of Computers*, 14(3):16–23, Jul-Sep 1997.

[Sav91] J. Savir. At Speed Test is not Necessarily an AC Test. In *Proceedings of The IEEE International Test Conference, ITC'91*, pages 722–728, 1991.

[SLAL94] T. Storey, C. Lapihuska, E. Atwood, and L.Su. A Test Methodology to Support an ASEM MCM Foundry. In *Proceedings of The IEEE International Test Conference, ITC'94*, pages 426–435, 1994.

[ZB97] Y. Zorian and H. Bederr. An Effective Multi-Chip BIST Scheme. *Journal of Electronic Testing: Theory and Applications*, 10:87–95, 1997.

[Zor94] Y. Zorian. A Structured Testability Approach for Multichip Modules Based on BIST and Boundary-Scan. *IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B*, 17(3):283–290, Aug 1994.

[Zor97a] Y. Zorian. Fundamentals of MCM Testing and Design-for-Testability. *Journal of Electronic Testing: Theory and Applications*, 10:7–14, 1997.