CMOS CURRENT-MODE HIGH-PRECISION EXPONENTIAL CIRCUIT WITH IMPROVED FREQUENCY RESPONSE

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Abstract: A new CMOS current-mode pseudo-exponential circuit based on the third-order Taylor series expansion will be presented. The advantage of the circuit with respect to the previous reported similar ones is the smaller value of the limited expansion error obtained by using a third-order approximation of the exponential function. The circuit presents the important advantage of independence of the output current on technological parameters. The frequency response of the circuit is improved due to the strong inversion operation of all MOS transistors. In order to evaluate the total error of the circuit core, the second-order effects have been taken into account, resulting an additional error summed to the error caused by the neglecting of the superior-order terms from the exponential function Taylor series expansion. The circuit area is relatively small due to the exclusively utilization of MOS transistors (all resistors have been removed from the circuit). The SPICE simulation of the circuit behavior confirms the theoretical estimated results.

Key words: exponential function, polynomial series, approximation error, frequency response.

1. INTRODUCTION

As an important part of CMOS VLSI computational area, the exponential circuits represent important building blocks for telecommunication applications, medical equipment, hearing aid and disk drives [1] - [5].

The exponential function could be easily obtained in the bipolar technology from the exponential characteristic [6] of the bipolar transistor. The nonzero value of the base current, especially for pnp transistors and the temperature dependence of the bipolar transistor parameters (the thermal voltage is linear increasing with temperature and the saturation current has an exponential dependence on temperature) introduces relatively large errors in the obtained exponential characteristic.

In CMOS technology, the exponential law is available only for the weak inversion operation of the MOS transistor. The great disadvantage of the computational circuits using MOS transistors in weak inversion is the poor circuit frequency response caused by the much smaller drain currents available for charge and discharge the parasite capacitances of the MOS devices. Thus, circuits realized in CMOS technology that require a good frequency response can be designed using only MOS transistors working in strong inversion (usually in saturation). In order to obtain the exponential function using the square characteristic of the MOS transistor in saturation, the original idea is to

approximate the exponential function with its $n-th$ order expansion (the polynomial series). The approximation error is proportional to the number of terms neglected in the expansion.

In this paper, an original CMOS VLSI current-mode pseudo-exponential circuit will be presented based on an excellent approximation of the exponential function by its third-order limited Taylor series expansion. The computed exponential function has the important advantage given by the independence of the output current on technological parameters.

2. THEORETICAL ANALYSIS

An original CMOS exponential circuit performing a very good frequency response, based exclusively on the quadratic characteristic of the MOS transistor in saturation and on a third-order limited expansion polynomial series will be further presented.

2.1. The third-order limited expansion polynomial series of the exponential function

In order to obtain the exponential function derived from the quadratic characteristic of the saturated MOS transistor, the original idea is to expand in Taylor series the exponential function (1) and to keep only the first n terms, the computing error caused by this limited series expansion being given by the remaining terms with an order greater than n (approximately, by the $(n+1)$-th order term).

$$\exp(x) = \sum_{k=0}^{\infty} \frac{x^k}{k!} \tag{1}$$

In this case, considering as variable the ratio of I_{IN} and I_O currents, where I_{IN} represents the input current and I_O is the reference current, the n-th order limited exponential function expansion series could be expressed as:

$$I_O \exp\left(\frac{I_{IN}}{I_O}\right) \cong I_O + I_{IN} + \frac{I_{IN}^2}{2I_O} + \frac{I_{IN}^3}{6I_O^2} + ... + \frac{I_{IN}^n}{(n!)I_O^{n-1}} \tag{2}$$

The new proposed circuit approximates the exponential function by its third-order expansion series and, in order to improve the circuit frequency response, it is based only at MOS transistors working in saturation. Thus, starting from the quadratic characteristic of the MOS device, it is necessary to implement two important functions: the squaring and the third-order current-mode functions.

2.2. The CMOS implementation of the squaring current-mode function

The original circuit for obtaining the squaring function uses four MOS transistors working in saturation, connected as it is shown in Figure 1.

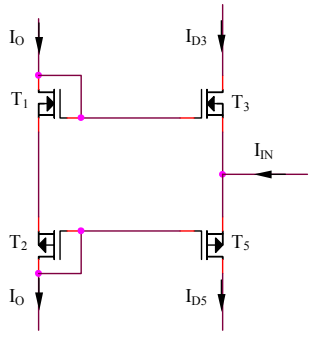

Figure 1 - The squaring current-mode function

Because $V_{GS_1} + V_{GS_2} = V_{GS_3} + V_{GS_5}$, it results:

$$2\sqrt{I_O} = \sqrt{I_{D_3}} + \sqrt{I_{D_5}} \tag{3}$$

equivalent to:

$$I_{D_3} = I_O - \frac{I_{IN}}{2} + \frac{I_{IN}^2}{16 I_O} \tag{4}$$

$$I_{D_5} = I_O + \frac{I_{IN}}{2} + \frac{I_{IN}^2}{16 I_O} \tag{5}$$

The quadratic term required from (2) will have the following linear expression:

$$\frac{I_{IN}^2}{I_O} = 8\left(I_{D_3} + I_{D_5}\right) - 16 I_O \tag{6}$$

2.3. The CMOS implementation of the third-order current-mode function

In order to obtain the third-order function using exclusively MOS transistors working in saturation, the new idea is to use the same circuit from Figure 1, having applied on its input changed values of the currents:

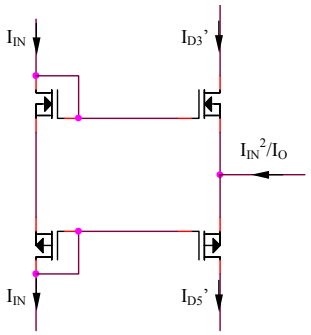

Figure 2 - The third-order current-mode function

In this case the drain current I_{D_3}' and I_{D_5}' will be:

$$I_{D_3}' = I_{IN} - \frac{I_{IN}^2}{2 I_O} + \frac{I_{IN}^3}{16 I_O^2} \tag{7}$$

$$I_{D_5}' = I_{IN} + \frac{I_{IN}^2}{2I_O} + \frac{I_{IN}^3}{16I_O^2} \tag{8}$$

resulting the following expression of the third-order term:

$$\frac{I_{IN}^3}{I_O^2} = 8\left(I_{D_3}' + I_{D_5}'\right) - 16I_{IN} \tag{9}$$

2.4. The CMOS implementation of the current-mode exponential circuit with third-order approximation

Considering the expressions (2), (6) and (9), the third-order approximation of the exponential function could be expressed as:

$$I_O \exp^{(III)}\left(\frac{I_{IN}}{I_O}\right) = 4\left(I_{D_3} + I_{D_5}\right) + \frac{4}{3}\left(I_{D_3}' + I_{D_5}'\right) - \frac{5}{3}I_{IN} - 7I_O \tag{10}$$

so a linear expression of the circuit currents, which can be implemented using multiple PMOS and NMOS current mirrors, resulting the following implementation of the third-order approximated exponential circuit:

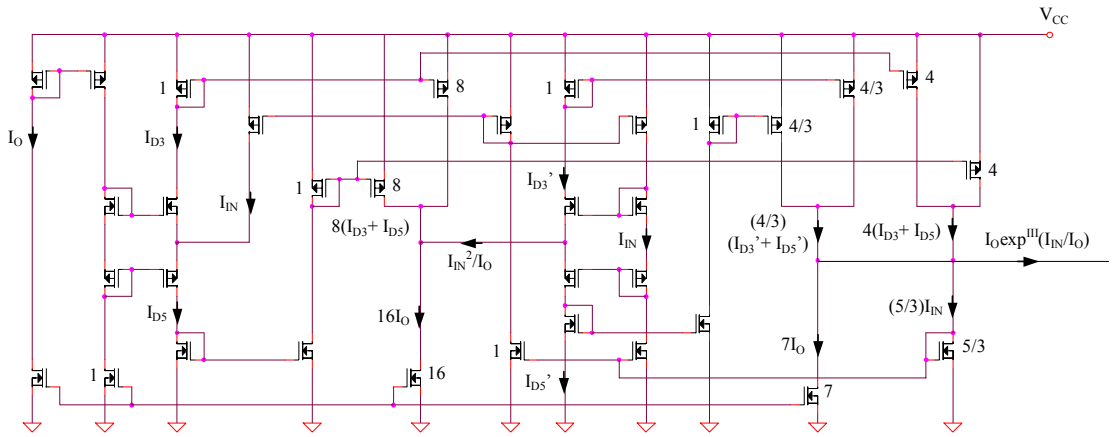

Figure 3 - The CMOS implementation of the current-mode exponential circuit with third-order approximation

2.5. Analysis of errors introduced by the second-order effects

All of the circuits presented above are affected by the second-order effects that degrade the quadratic law of the MOS transistor. These undesired effects are modeled by the following relations (short channel effect (11) and mobility degradation (12)).

$$I_D = \frac{K}{2}\left(V_{GS} - V_T\right)^2\left(1 + \lambda V_{DS}\right) \tag{11}$$

$$K = \frac{K_0}{\left[1 + \theta_G\left(V_{GS} - V_T\right)\right]\left(1 + \theta_D V_{DS}\right)} \tag{12}$$

Considering that the design condition $\lambda = \theta_D$ is fulfilled, the gate-source voltage of a MOS transistor working in saturation at a drain current I_D will be:

$$V_{GS} = V_T + \sqrt{\frac{2I_D}{K}} + \theta_G \frac{I_D}{K} \tag{13}$$

Taking into account the second-order effects, the approximated expression (10) of the exponential function will be affected also by an error caused by these undesired effects.

In conclusion, the circuit total error will be the sum of two components: first, given by the limited Taylor expansion series, proportional to the number of terms neglected in the expansion and second, produced by the second-order effects that affect the MOS transistor operation.

3. EXPERIMENTAL RESULTS

The SPICE simulation of the circuit core (the voltage squarer) is presented in Figure 4, confirming the theoretical estimated results.

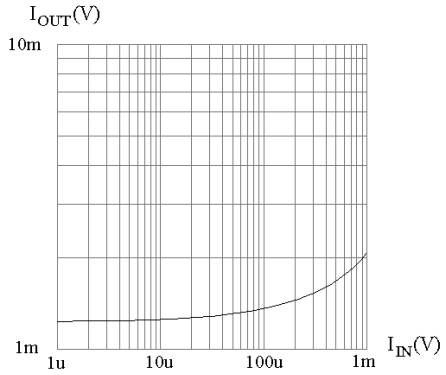

Figure 4 - The SPICE simulation of the current squarer

4. CONCLUSIONS

A CMOS current-mode pseudo-exponential circuit based on the third-order limited expansion Taylor series has been presented. The advantage of the circuit with respect to the previous reported similar ones is the smaller value of the limited expansion error due to the third-order approximation of the exponential function. The circuit presents the important advantage of the independence of the output current on technological parameters. The frequency response of the circuit was improved due to the strong inversion operation of all MOS transistors. In order to evaluate the total error of approximating $\exp(x)$ function, the second-order effects were taken into account, resulting an additional error summed to the error caused by the limited Taylor series expansion. The circuit area has a relatively small value due to the exclusively utilization of MOS transistors (without any resistor). The SPICE simulation of the circuit behavior confirms the theoretical estimated results.

5. REFERENCES

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