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SIMULATION AND ANALYSIS TECHNIQUES OF NONLINEARITY EFFECTS IN HIGH PERFORMANCE ADCS

Ana Rusu & Hannu Tenhunen

Royal Institute of Technology
Laboratory of Electronic and Computer Systems/ESDLab
Department of Microelectronics and Information Technology
Electrum 229, SE-164 40 Kista, Sweden
Tel: 08-790 4174
E-mail: ana@imit.kth.se, hannu@imit.kth.se

Abstract: Oversampled sigma-delta modulators and pipelined architectures are the most suitable candidates to meet the needs of signal wideband and high dynamic range for communication applications. This paper presents how oversampling, sigma-delta modulation and pipeline concept can be employed in analog-to digital conversion to extend the signal bandwidth into the range of several megahertz and the dynamic range in excess of 16 bits. We purpose a new approach for wideband and high-resolution analog-to-digital converters design and some of specific simulation and analysis issues for nonlinearity effects.

Keywords: sigma-delta modulation, pipeline concept.

1. INTRODUCTION

Transceivers for future digital communications applications need to be portable, battery-powered, wireless and multi-bands. Today's single chip solutions for RF front-ends do not yield complete system integration. For example, they typically still need external components for impedance match, for antenna switches, for power amplifiers and for RF bandpass filters. These goals can be achieved by converting analog signals into digital as close as possible to the antenna and performing most of the processing in the digital domain. In this way, expensive discrete filters are replaced with low-complexity analog integrated filters and the task of accurate and high-selectivity filtering is turn to digital filters. The programmability of digital filters offers the capability to support the variety of telecommunication standards for multimode radio receivers. However, the trend toward increased digital signal processing also increases the dynamic range and bandwidth required of the analog-to-digital interfaces. The performance of a multi-standard receiver is directly influenced by the performance of the ADC. This leads to more and more demanding specifications for the required A/D converters. Thus there is an urgent need to research and develop techniques for the high-speed high-resolution data converters. In recent years, among the wide variety of ADC architectures, sigma-delta and pipelined converters are the most suitable candidates to meet the needs of signal wideband and high dynamic range, [1], [2].

A sigma-delta converter can provide a high-resolution conversion and high linearity using single-bit implementations. Unfortunately, these converters required a high oversampling ratio and than an MHz signal bandwidth is extremely difficult to achieve. Solution to increase signal bandwidth is to reduce oversampling ratio (OSR), but it is necessary to provide additional reduction of in-band quantization noise by using a multi-bit architecture. A multi-bit sigma-delta modulator has the advantage of a better stability with more aggressive noise transfer function designs and also reduced decimation filter complexity and reduced power consumption. This can be achieved by using high-order multi-bit modulator loops with multi-bit feedback linearized DAC or with a truncation feedback signal. Another solution is cascaded sigma-delta modulator. Unfortunately, the feedback multi-bit DAC are not inherently linear as single-bit architecture and than need DAC linearization techniques.

Pipelined ADCs are more commonly used to realize high conversion rates since they provide effective signal bandwidth equal to a half of sampling frequency. A pipelined topology is implemented with a multiple small ADC and there are more efficient than a single large ADC. The limitations of pipelined ADC are the dynamic range and DAC non-linearity. Compensation for non-linearity is possible using analog or digital calibration or mismatch shaping techniques. The pipelined ADC sensitivity to component mismatches results in a significant increase in complexity and power dissipation.

Current publications and results show that the multi-bit sigma-delta ADC topologies combined with pipelined architectures are appropriate for wideband applications [3], [4], [5]. In [3] was proposed a cascaded multi-bit sigma-delta pipeline ADC. Idea consist of cascades a sigma-delta modulator with additional stages of quantization. Thus, the high conversion rate of a pipelined quantizer is combined with the wide dynamic range of a high-order multi-bit sigma-delta modulator. In [4], the author has been proposed new high-performance sigma-delta modulator topologies based on feedforward signal path implementation, residue-compensated concept and pipeline topology. In [5], the authors have been introduced the analog-to-digital conversion by performing spatial oversampling in a sigma-delta topology. A new approach capable of providing good enough performance is to oversample a standard pipeline A/D converter, and shape the mismatch out of band, which will be removed by a digital filter, [6]. In context of wideband applications, circuit and layout design issues start to become critical and new design techniques are required to solve the problems as jitter, nonlinearity and intermodulation distortion.

We believe that more efficient approach for wideband and high-resolution A/D conversion would be oversampling techniques and a new sigma-delta topology with feedforward path combined with temporal and spatial pipelining concept.

2. PROPOSED TOPOLOGY

The resolution of the sigma-delta modulator is predominantly governed by the order of the modulator, number of bits used in quantizer and the oversampling ratio. One attractive way to increase the dynamic range is to use a multi-bit quantizer. Thus for a given resolution, the use of multi-bit quantizer can reduce the OSR for wideband A/D converters. The use of multi-bit quantizer, however, introduces nonlinearity error from the feedback multi-bit DAC. Such error is not noise shaped in frequency by the forward path of the modulator and appears at the modulator output. As such, the linearity of the sigma-delta modulator depends on the linearity of the DAC in the

feedback path. To mitigate this problem, interpolation, dynamic element matching, element-trimming and digital-correction techniques have been used for the feedback DAC compensation, [4]. Thus high dynamic range A/D converter implies increasing the cost of the ADC, as component precision in the feedback DAC should equal the overall converter resolution. Such problem can be alleviated by introducing a multi-bit topology with feedforward path, which has reduced sensitivity to opamp nonlinearities [7]. This topology uses only one DAC in the feedback path and than the complexity of circuit and chip area decreases. In the multibit sigma-delta modulator with feedforward path the nonlinearity problem is achieved by making signal transfer function, STF (z)=1. Another advantage of this topology is that the integrators process quantization noise only and than their performance requirements are relaxed.

Our approach for wideband ADC design uses the sigma-delta modulator with feedforward path, shown in Fig. 1. in a temporal pipeline topology, shown in Fig.2. The proposed topology combines the advantage of sigma-delta modulator with feedforward path and pipeline concept to achieve high dynamic range and wideband A/D conversion. The block diagram of the pipelined sigma-delta modulator is shown in Fig. 3, where the first two stages are second-order sigma-delta modulators with feedforward path and the last stage is a flash ADC.

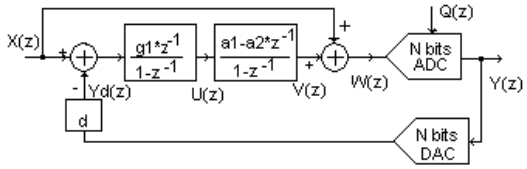


Fig. 1. A multi-bit sigma-delta modulator with feedforward path

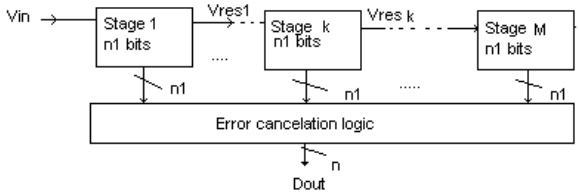


Fig.2. A pipelined ADC topology

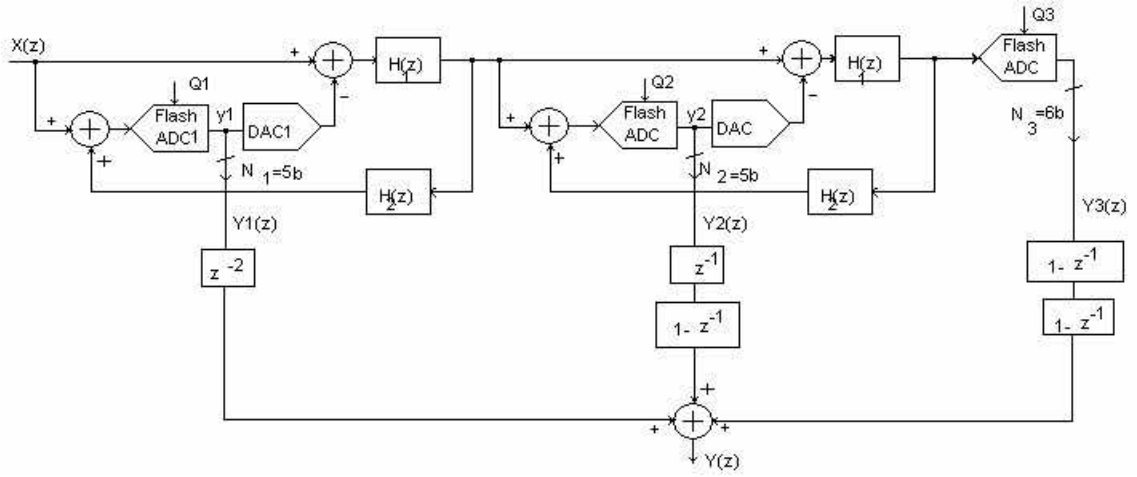


Fig. 3. A 5 bit-5 bit-6 bit pipelined sigma-delta modulator

As shown in Fig. 3., the input X(z) enters in the first sigma-delta loop whose 5-bit quantizer introduces a quantization error Q_1. The output of the first integrator from the first stage is the input for the second stage. The 5-bit quantizer from the second stage introduces the quantization error Q_2. The output of the first integrator from the second

stage is the input for the flash ADC. The 6-bit quantizer from the third stage introduces the quantization error Q_3. The outputs of these three-pipelined stages are combined as shown in Fig. 3. to cancel the quantization noise from the first and second stage and to produce the digital output. For simplicity, in the linear model it is assumed that the integrators are ideal and than the stage outputs are:

$$Y_1(z) = X(z) + \frac{1}{1+H_1(z)H_2(z)} Q_1(z) \tag{1}$$

$$Y_2(z) = -\frac{H_1(z)}{1+H_1(z)H_2(z)} Q_1(z) + \frac{1}{1+H_1(z)H_2(z)} Q_2(z) \tag{2}$$

$$Y_3(z) = -\frac{H_1(z)}{1+H_1(z)H_2(z)} Q_2(z) + Q_3(z) \tag{3}$$

These three outputs are processed digitally to remove the flash quantization errors $Q_1(z)$ and $Q_2(z)$ and to obtain a more accurate digital estimate of the input signal X(z). The quantization errors $Q_1(z)$ and $Q_2(z)$ are digitally filtered with a transfer function $H_d(z)$ and $(H_d(z))^2$ respectively. The output Y(z) of the overall modulator after digital cancellation is:

$$Y(z) = z^{-2} Y_1(z) + z^{-1} H_d(z) Y_2(z) + (H_d(z))^2 Q_3(z) \tag{4}$$

$$\begin{aligned} Y(z) = {} & z^{-2} \cdot X(z) + \frac{z^{-1}}{1+H_1(z)H_2(z)} \cdot \left(z^{-1} - H_1(z) \cdot H_d(z)\right) \cdot Q_1(z) + \\ & \frac{H_d(z)}{1+H_1(z)H_2(z)} \cdot \left(z^{-1} - H_1(z) \cdot H_d(z)\right) \cdot Q_2(z) + (H_d(z))^2 \cdot Q_3(z) \end{aligned} \tag{5}$$

If the digital transfer function $H_d(z)$ in (5) is identical to $(1-z^{-1})$ (i.e., $H_d(z)= z^{-1}/H_1(z)$), then the output becomes:

$$Y(z) = z^{-2} X(z) + (1 - z^{-1})^2 \cdot Q_3(z) \tag{6}$$

It is seen that the input signal is delayed by an amount equal to z^{-2} and the multi-bit quantization error of the last stage is shaped by the function function $(1-z^{-1})^2$.

3. SIMULATION AND ANALYSIS

The model used for simulation includes the circuit nonidealities in order to evaluate their impact on the overall performance of the modulator. The integrator was implemented using an opamp with a finite gain $A_d = 1/(1-\alpha)$. The variable α controls the integrator leakage from the finite gain of the opamp. The multibit quantizer is a flash A/D converter that consists of a resistive divider ladder followed by a bank of ideal comparators. The D/A converter from the feedback path is a scaled converter whose unit-elements are controlled by the 'da_error' variable. This variable is used to evaluate the effect of the DAC impairments on the spectrum.

The proposed topology has been simulated in MATLAB. For simulation the pipelined topology is a 5b-5b-6b configuration. The opamp gain used to construct the integrator is 46dB and the feedback DAC has a mismatch error of 0.001%.

The noise sources which contribute to the overall noise performance of this topology are: the quantization noise of the third stage Q3, the quantization noise leakage of the first stage Q_1, the quantization noise leakage of the second stage Q_2, noise energy of capacitor mismatch errors in DAC1 and DAC2 and noise devices. In this paper we analyze the effects of capacitor mismatch error on the noise performance. The unit-elements of DAC are assigned a Gaussian distribution with a standard deviation of 'da_error'.

Spectral analysis method generally uses the single tone mode, when a sine wave is applied to the converter analog input. Fig. 4 shows the output spectrum in the single-tone mode, for an input signal with 3 MHz frequency and –6dB amplitude bellow full scale, the sampling frequency of 160MHz and OSR of 8. The output spectrums were computed using 16384 points FFT.

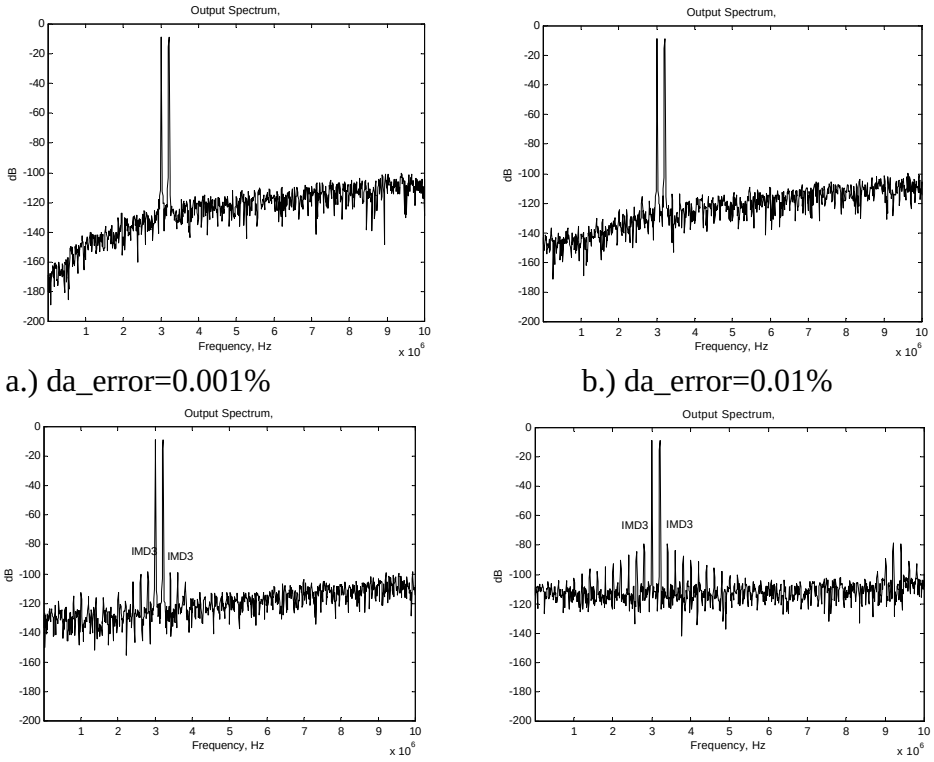
For data converters for communication applications, characterized by both high resolution and high-speed conversion the test method are based on "two-tone" intermodulation test [9]. Intermodulation distortion occurs when the non-linearity of a device or system with multiple input frequencies causes undesired outputs at other frequencies. In a communications system this means that signals in one channel can cause interference with adjacent channels. As the spectrum becomes busier and the channels become more tightly spaced, minimizing intermodulation distortion becomes more important. A convenient way to analyze IMD is to combine two equal power signals with a set frequency spacing at the input of the modulator. The modeling can be accomplished with a single two-tone signal consisting of two sinewaves of the same amplitude and approximately equal frequency, f_1 and f_2 [10]. For the input signal:

$$V_{in}(t) = \frac{A}{2}\left[\sin(2\pi f_1 t + \phi_1) + \sin(2\pi f_2 t + \phi_2)\right] \quad (7)$$

result the following distortion lines:

- Intermodulation distortion:
  2^{nd} order: IMD($f_1 \pm f_2$) ; 3^{rd} order: IMD($2f_1 \pm f_2$); IMD($2f_2 \pm f_1$)
- Harmonic distortion:
  2^{nd} order: HD($2f_1$); HD($2f_2$); 3^{rd} order: HD($3f_1$); HD($3f_2$)

Using this test method we have been evaluate the influence of the DAC nonlinearity on the intermodulation distortion.



a.) da_error=0.001% b.) da_error=0.01%

c.) da_error=0.1% d.) da_error=1%

Fig. 4. Two-tone intermodulation test

Fig. 4 shows the spectrum of the proposed topology with two high frequency tones at 3MHz and 3.2MHz applied to the input of modulator. In the first plot (a) where the DAC is ideal, the spectrum does not uncover any impairment. In the next plots (b,c,d) extra low frequency noise and intermodulation products are clearly visible as a result of the DAC impairments. The resulting third-order intermodulation distortion products are –102 dB bellow the amplitude of the two input tones for DAC mismatch errors of 0.01%, –87 dB for 0.1% and –70 dB for 1%. These results show the effects of DAC impairments on the dynamic performances and can be used to design the feedback DACs and to choose the linearization technique.

4. CONCLUSIONS

This work demonstrates that pipelined sigma-delta modulation is a viable option for the high-resolution digitization of megahertz bandwidth signal. For the proposed topology using a multibit quantizer, the OSR requirement is reduced and than we can obtain a wideband ADC. High performance can achieve by using a combination of sigma-delta modulator with feedforward path and pipelined concept. Pipelining decouples the conversion rate from the conversion time, so that it is possible to achieve high-speed operation. The simulation results using two-tone intermodulation test show the harmonic distortion and intermodulation distortion caused by the DAC nonlinearity. The use of high linearity DAC in the feedback path is not necessary.

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