CMOS LINEARIZED DIFFERENTIAL AMPLIFIERS USING STRONG INVERSION AND BULK-DRIVEN MOS TRANSISTORS

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Abstract: Two CMOS differential amplifiers using MOS transistors in saturation and in weak inversion will be presented. An original linearization technique based on a parallel connection of two differential stages opposite- excited and different-polarized will be implemented. The canceling of the third-order term from the output voltage expression allows obtaining a reduction of the distortion coefficient with about an order of magnitude for both differential amplifiers. The weak-inversion circuit presents the advantage of a very small current consumption, making it compatible with low-power designs. The SPICE simulation confirms the theoretical estimated linearity improvement.

Key words: linearity, second-order effects, silicon area.

1. INTRODUCTION

The CMOS differential amplifiers find applications in operational amplifiers, voltage comparators, voltage references, video amplifiers, modulators and demodulators or A/D and D/A converters. Because of the fundamental nonlinear characteristic of MOS transistors, the linearity of the differential amplifier is limited, resulting the possibility of achieving small distortions only for a restricted input voltage range (the amplitude of the input voltage for the classic differential amplifier using MOS transistors in saturation have to be below a few hundreds of mV). It is obviously the necessity of implementing a linearization technique for decreasing the superior-order nonlinearities of the MOS differential stage and for increasing the available range for the input voltage amplitudes. An important goal of low-power designs is represented by the circuit current consumption. Usually supplied from batteries (portable devices [1], [2], medical equipments [3]), the power requirements of the differential amplifier must be as small as possible. Classical designs using MOS transistors in saturation have a relatively large current consumption and there are not indicated for low-power applications, but they present the advantage of a much better frequency response. The newest approaches of low-power CMOS circuits exploit the subthreshold operation of the MOS transistor due to the very small value of the drain current in this region [4].

This paper presents two differential amplifiers using MOS transistors in saturation and subthreshold region, designed for good frequency response and low-power applications, respectively. The proposed linearization technique is based on a parallel connection of two quasi-identical differential amplifiers, which assures the canceling of the

third-order distortions from the output voltage expression. The double drive of the weak-inversion differential amplifier (on gate and on bulk) modifies the design condition for canceling the third-order distortions by introducing desired and controllable small asymmetries in the differential amplifiers' parameters.

2. THEORETICAL ANALYSIS

2.1. The differential amplifiers using MOS transistors in saturation

The classical approach of a CMOS differential amplifier is based on MOS transistors in saturation. Because of the quadratic law, which describes this region of operation, the circuit linearity will be relatively poor, affected by the odd-order distortions, mainly represented by the third-order ones. Additionally, the large values of the circuit current consumption, typically in the miliamperes range, make it incompatible with low-power designs, but assure a good frequency response of the differential amplifier.

2.1.1. The classical differential amplifier using MOS transistors in saturation

The expressions of drain currents for the MOS differential amplifier with transistors in saturation are given by:

$$I_{1,2} = \frac{I_0}{2} \pm \frac{I_0}{2}\left(\frac{Kv_{id}^2}{I_0} - \frac{K^2 v_{id}^4}{4I_0^2}\right)^{1/2} \tag{1}$$

having the following expansion in polynomial series, limited to the fifth-order term:

$$I_{1,2}(v_{id}) = \frac{I_0}{2} \pm \frac{K^{1/2} I_0^{1/2}}{2} v_{id} \mp \frac{K^{3/2}}{16 I_0^{1/2}} v_{id}^3 \mp \frac{K^{5/2}}{256 I_0^{3/2}} v_{id}^5 \tag{2}$$

v_{id} is the differential input voltage, I_0 is the polarization current of the circuit and K is the transconductance parameter from the MOS transistor model. The total harmonic distortions coefficient (approximated with the third-order one) will be $THD_3 \cong KV_{ID}^2 / 8I_0$. In conclusion, the circuit linearity is rather poor, especially for large values of the input voltage.

2.1.2. The linearization technique for CMOS differential amplifier using MOS transistors in saturation

In order to improve the circuit linearity, two parallel-connected quasi-identical opposite-excited differential amplifiers (Figure 1) could be used for canceling the third-order term from the circuit transfer function, equivalent with an important reduction of the circuit distortions.

The differential amplifier output current expression is:

$$I_o \cong (I_{1a} - I_{2a}) - (I_{1b} - I_{2b}) = \left(K_a^{1/2} I_{0a}^{1/2} - K_b^{1/2} I_{0b}^{1/2}\right) v_{id} - \\ - \frac{K_a^{3/2} I_{0a}^{-1/2} - K_b^{3/2} I_{0b}^{-1/2}}{8} v_{id}^3 - \frac{K_a^{5/2} I_{0a}^{-3/2} - K_b^{5/2} I_{0b}^{-3/2}}{128} v_{id}^5 \tag{3}$$

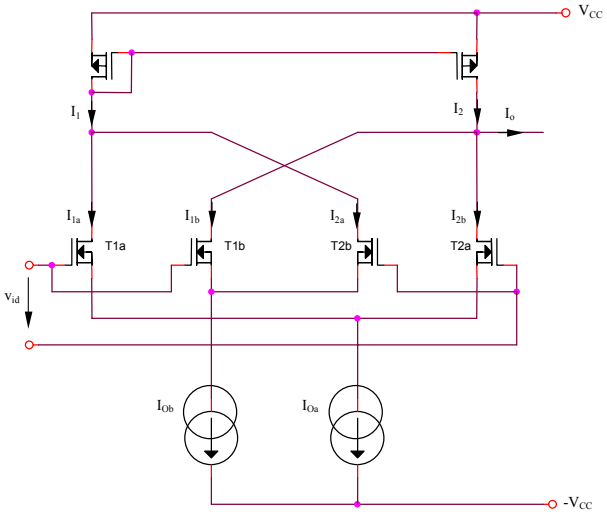

Figure 1 - The linearized differential amplifier using MOS transistors in saturation

So, the condition of removing the third-order term from I_0 expression is $I_{0a}/I_{0b} = (K_a/K_b)^3$, resulting $I_O \cong a_1 v_{id} + a_5 v_{id}^5$, where a_1 and a_5 are constant coefficients:

$$a_1 = K_a^{1/2} I_{0a}^{1/2} \left[1 - \left(\frac{K_b}{K_a}\right)^{2/3}\right]; \quad a_5 = \frac{1}{128} \frac{K_a^{5/2}}{I_{0a}^{3/2}} \left[1 - \left(\frac{K_a}{K_b}\right)^{2/3}\right] \tag{4}$$

equivalent with a total harmonic distortion coefficient (mainly caused by the fifth-order term) equal with:

$$THD_5 = \frac{1}{128} \left(\frac{K_a}{I_{0a}}\right)^2 \left(\frac{K_a}{K_b}\right)^2 V_{ID}^4 \tag{5}$$

Considering small asymmetries between the parallel-connected differential amplifiers from Figure 1 and supposing that the two current sources I_{0a} and I_{0b} are implemented as simple current mirrors using $T_{3a} - T_{3b}$ and $T_{4a} - T_{4b}$ transistors, the improvement in linearity for the previous presented technique is:

$$\frac{THD_3}{THD_5} = 8 \left(\frac{V_{GS_{3a}} - V_T}{V_{ID}}\right)^2 \tag{6}$$

that is proportional with the square-ratio of the effective gate-source voltage for transistors from the current mirror and the magnitude of the differential input voltage.

2.2. The bulk-driven weak inversion MOS differential amplifier

Another approach of the CMOS differential amplifier, designed for low-power applications, uses MOS transistors operating in subthreshold region. The advantage is the possibility of a double drive of the transistor, on gate and on bulk, correlated with the low-power consumption.

2.2.1. The simple bulk-driven weak inversion MOS differential amplifier

The expressions of drain currents for the MOS differential amplifier with transistors in weak inversion are:

$$I_{1,2} = \frac{I_0}{1+\exp\left(\pm\frac{V_{GS_1}-V_{GS_2}}{nV_t}\right)\exp\left(\pm\frac{n-1}{n}\frac{V_{BS_1}-V_{BS_2}}{V_t}\right)} \tag{7}$$

where n is a constant parameter depending on the technology, $V_t = KT/q$ is the thermal voltage and V_{GS} and V_{BS} are the gate-source and bulk-source voltage. Considering passive bulks, equivalent with $V_{BS_1} = V_{BS_2} = 0$ and $V_{GS_1} - V_{GS_2} = v_{id}$, it results a total harmonic distortion coefficient (mainly caused by the third-order harmonic) equal to:

$$THD_3' = \frac{V_{ID}^2}{12n^2V_t^2} \tag{8}$$

So, it is necessary to develop a linearization technique for reducing the circuit distortions.

2.2.2. Linearization technique for the bulk-driven weak inversion MOS differential amplifier

It will be proposed a new linearization technique for a weak inversion MOS differential amplifier, based on a parallel connection of two quasi-identical stages opposite-excited and different-polarized. Each differential amplifier is driven with two input voltages: v_{id} on gate and $A_{a(b)}v_{id}$ on bulk. The advantage of the double drive is the introducing of additional controllable asymmetries between these stages by a proper choice of $A_{a(b)}$ voltage gains, in order to obtain a simple design condition for canceling the third-order distortions of the entire differential amplifier. The circuit of the linearized differential amplifier using subthreshold-operated MOS transistors is presented in Figure 2.

The drain currents of the MOS transistors have the following expressions:

$$I_{1,2a(b)} = \frac{I_{0a(b)}}{1+\exp\left(\pm K_{a(b)}\frac{v_{id}}{V_t}\right)} \tag{9}$$

where $K_{a(b)} = \left[1+(n-1)A_{a(b)}\right]/n$. In order to improve the circuit linearity, a fifth-order limited polynomial series of the exponential function will be considered:

$$\exp(x) \cong \frac{1}{2} - \frac{x}{4} + \frac{x^3}{48} - \frac{x^5}{480} \tag{10}$$

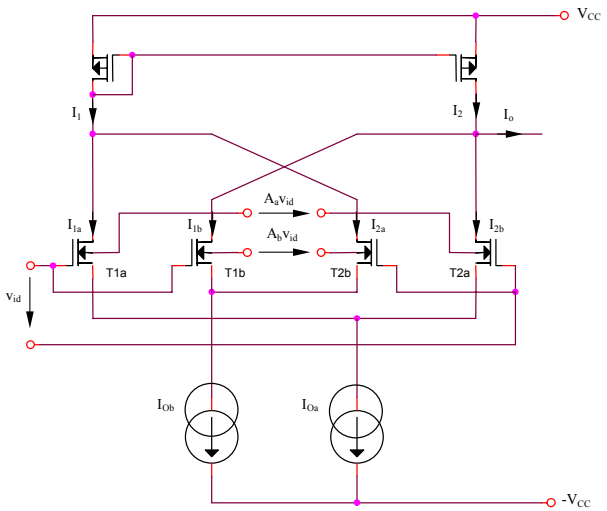

Figure 2 - Linearization technique for the bulk-driven MOS differential amplifier

Using this expansion, the expression of the output current for the entire differential amplifier $T_{1a} - T_{1b} - T_{2a} - T_{2b}$ will be:

$$I_o = (I_{1a} - I_{2a}) - (I_{1b} - I_{2b}) = \frac{K_a I_{0a} - K_b I_{0b}}{2V_t} v_{id} - \frac{K_a^3 I_{0a} - K_b^3 I_{0b}}{24V_t^3} v_{id}^3 + \frac{K_a^5 I_{0a} - K_b^5 I_{0b}}{240V_t^5} v_{id}^5 \quad (11)$$

In order to cancel the main non-linearity of the circuit, the new idea is to cancel the third-order term from expression (11) of the output current. So, the design condition is:

$$\frac{K_a}{K_b} = \sqrt[3]{\frac{I_{0_b}}{I_{0_a}}} = \frac{1+(n-1)A_a}{1+(n-1)A_b} \quad (12)$$

resulting a general expression of I_o current given by $I_o \cong a_1 v_{id} + a_5 v_{id}^5$. The constants a_1 and a_5 have the following expressions:

$$a_1 = \frac{K_a}{2V_t} I_{0a} \left[1 - \left(\frac{I_{0b}}{I_{0a}}\right)^{2/3}\right]; \quad a_5 = \frac{K_a^5}{240V_t^5} I_{0a} \left[1 - \left(\frac{I_{0b}}{I_{0a}}\right)^{-2/3}\right] \quad (13)$$

After applying the described linearization technique, the total harmonic distortion coefficient (mainly caused by the fifth-order harmonic) will be:

$$THD_5' = \frac{V_{ID}^4}{120(nV_t)^4} [1+(n-1)A_a]^2 [1+(n-1)A_b]^2 \quad (14)$$

So, it is possible to obtain an important reduction of THD using this technique. The small asymmetry between the two parallel-connected differential amplifiers is obtained both by a different polarization current $I_{a(b)}$ and by a different bulk drive voltage, $A_{a(b)} v_{id}$.

3. EXPERIMENTAL RESULTS

The circuits were implemented in $0.35\mu m$ CMOS technology. The SPICE simulation for verifying the circuit linearity confirms the theoretical estimations. Ten characteristics of the bulk-driven weak-inversion differential amplifier for different polarization currents are presented in Figure 3.

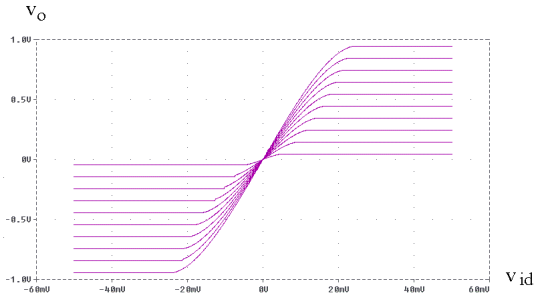

Figure 3 - The SPICE simulation for the bulk-driven CMOS differential amplifier

4. CONCLUSIONS

A new linearization technique for CMOS differential amplifier based on a parallel connection of two quasi-identical differential stages opposite-excited and different-polarized was presented. The canceling of the third-order term from the output voltage expression assures a reduction of the total harmonic distortions coefficient with respect to the basic circuit with about an order of magnitude. For obtaining a low-power operation of the CMOS differential amplifier, the MOS transistors were polarizated in the subthreshold region, resulting a very small current consumption. The double drive of this circuit (on gate and on bulk) modifies the design condition for canceling the third-order distortions by introducing desired small asymmetries in the two parallel-connected differential amplifiers.

The SPICE simulation confirms the theoretical estimated circuit linearity improvement.

5. REFERENCES

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