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LOW-AREA CMOS ACTIVE RESISTOR INDEPENDENT ON THE BULK EFFECT

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Abstract: *This paper presents a new linearity improvement technique for a CMOS active resistor. In order to minimize the silicon occupied area, an original method will be designed, having the result of about two order of magnitude reducing area with respect to a classical resistor. The circuit theoretical estimated linearity error is 0.35% for an input range of ±500mV , confirmed by SPICE simulations. The circuit is designed for low-voltage low-power application (a supply voltage of about ±3.3V) and it is implemented in 0.35μm CMOS technology. The layout area (60μm×80μm) is minimized using an original technique based on an optimal implementation of the current-controlled voltage generators from the active resistor circuit.*

Key words: linearity, second-order effects, silicon area

1. INTRODUCTION

CMOS active resistors are extensively used in analog integrated circuits for replacing the large value passive resistors, having the great advantage of a much smaller area occupied on silicon. Their utilisation domains includes amplitude control in low distortion oscillators, voltage controlled amplifiers and active RC filters. This wide range of applications for programmable floating resistors has stimulated a significant research effort for linearising MOS transistor characteristics.

The first generation of MOS active resistors [1], [2] used MOS transistors working in the linear region. The main disadvantage is that the realised active resistor is inherently nonlinear and the distortion components were complex functions on MOS technological parameters.

A better design of CMOS active resistors is based on MOS transistors working in saturation [3], [4], [5]. Because of the quadratic characteristic of the MOS transistor, some linearisation techniques were developed in order to minimize the nonlinear terms from the current-voltage characteristic of the active resistor. Usually, the resulting linearisation of the $I-V$ characteristic is obtained by a first-order analysis. However, the second-order effects which affect the MOS transistor operation (mobility degradation, bulk effect and short-channel effect) limits the circuit linearity introducing odd and even-order distortions, as shown in [4].

2. THEORETICAL ANALYSIS

The simplified schematic of the proposed CMOS active resistor is presented in Figure 1. V_X and V_Y are the output pins of the active resistor, I_{XY} is the current through the circuit, V_C is a DC potential which fix the value of the equivalent resistance between X and Y pins and sets the I_{D_7} and I_{D_8} current to be equal to I_O current. V_O generators are voltage sources controlled by the current I_O; their implementation will be further analyzed. I_1, I_2, I and I' are intern currents of the active resistor.

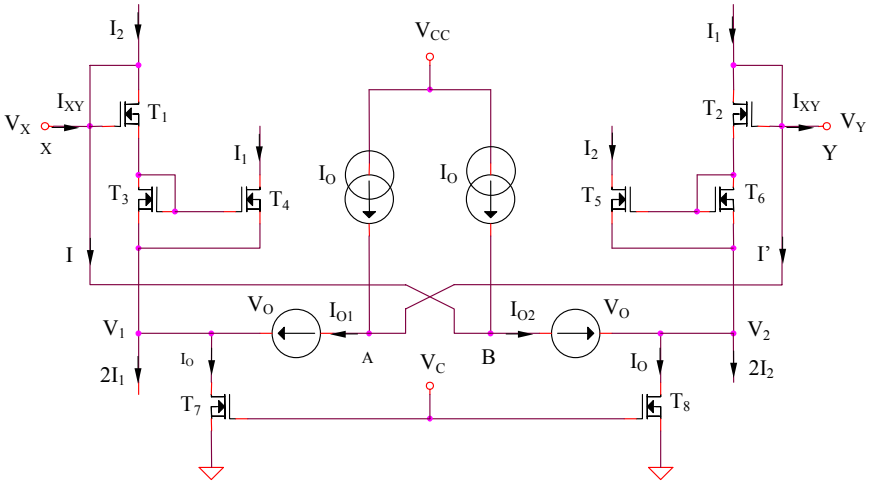

Figure 1: Simplified schematic of the CMOS active resistor

2.1. First-order analysis

It will be demonstrated that the circuit presented in Figure 1 is functionally equivalent to a classical resistor between V_X and V_Y output pins, that is $V_X - V_Y = R_{ech.} I_{XY}$, where $R_{ech.}$ represents the equivalent resistance of the circuit. Considering that all MOS transistors are working in saturation, characterized by the first-order simplified quadratic law $I_D = (K/2)(V_{GS} - V_T)^2$, the sum and the difference between the two gate-source voltages V_{GS_1} and V_{GS_2} are $V_{GS_1} + V_{GS_2} = 2V_O$ and $V_{GS_1} - V_{GS_2} = 2(V_X - V_Y)$, respectively. It results:

$$R_{ech.} = \frac{1}{2K(V_O - V_T)} \tag{1}$$

I_O and V_O are current and voltage generators, respectively. The implementation of the voltage sources V_O is correlated with the necessity of removing the dependence of the circuit equivalent resistance $R_{ech.}$ on the threshold voltage V_T, with the result of the bulk effect independence. The new proposed idea is to implement these voltage sources as sums of n gate-source voltages of MOS transistors having the aspect ratio (W/L) $m-th$ time greater than the others transistors from Figure 1. This original implementation is presented in Figure 2.

In this case, V_O voltage could be written as $V_O = n(V_T + \sqrt{2I_O / mK})$. Using that the control potential V_C is $V_C = V_T + \sqrt{2I_O / K}$, it results the following expression of the equivalent resistance:

$$R_{ech.} = \frac{1}{2K\left[\left(n - 1 - \frac{n}{\sqrt{m}}\right)V_T + \frac{n}{\sqrt{m}}V_C\right]} \tag{2}$$

The increasing of the circuit linearity is achieved by removing the dependence of $R_{ech.}$ on V_T. It results $m = n^2/(n-1)^2$.

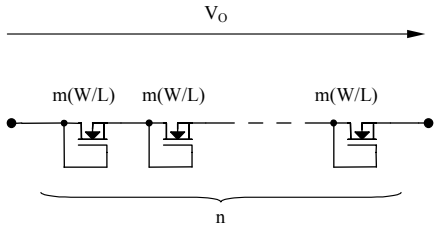

Figure 2: The original design of V_O voltage sources for removing the bulk effect

and $V_O = V_T + (n-1)V_C$. The equivalent resistance will be $R_{ech.} = 1/[2K(n-1)V_C]$.

A very important goal in VLSI design and especially in active resistors design is the minimization of the circuit area. Because the active resistor area except the implementation of V_O sources is imposed by the proposed principle of operation, it is necessary to find the optimal pair (m, n), which assures the minimization of the V_O area. A_{V_O} is directly proportional with the following function:

$$f(m,n) = mn = \frac{n^3}{(n-1)^2} = f(n) \tag{3}$$

The dependence $f(n)$ is presented in Figure 3.

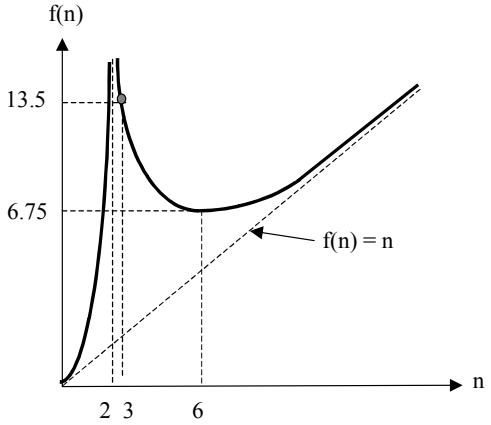

Figure 3: The $f(n)$ function

A_{V_O} will have a minimal value for $n = 6$, that is for a particular implementation of V_O sources using 6 MOS transistors with aspect ratios $2.25 - th$ greater than the

other transistors from Figure 1. Because when n increases, the decreasing of R_{ech} has a more important impact than the area reduction A_{V_O}, the better realization of V_O must include three MOS transistors for each V_O generator. In this case, the most important value of the area reduction with respect to a classical resistor could be obtained.

In the following table, A_{ct} represents the area of all MOS transistors from the circuit full implementation (Figure 4) of the active resistor, except transistors from the V_O sources, A_{V_O} is the area of MOS transistors from V_O generators, A_{tot} is the total area occupied by the active resistor from the Figure 4, A_{clas} represents the area of a classical resistor with a resistance equal to R_{ech} and f is the area reduction factor (using the active resistor to replace the classic resistor).

(n,m)	***(3; 9)***	***(4, 4)***	***(6; 2.25)***
$A_{ct}\,(\mu m^2)$	23×4	23×4	23×4
$A_{Vo}\,(\mu m^2)$	54×4	32×4	27×4
$A_{tot}\,(\mu m^2)$	77×4	55×4	50×4
$R_{ech.}$	$2/(KV_C) = 40\ k\Omega$	$1/(KV_C) = 20\ k\Omega$	$1/(2KV_C) = 10\ k\Omega$
$A_{clas}\,(\mu m^2)$	20 000	10 000	5 000
$f = A_{clas} / A_{tot}$	65	45	25

The complete circuit implementation is presented in Figure 4. V_C is an externally applied potential used to control the value of the equivalent resistance.

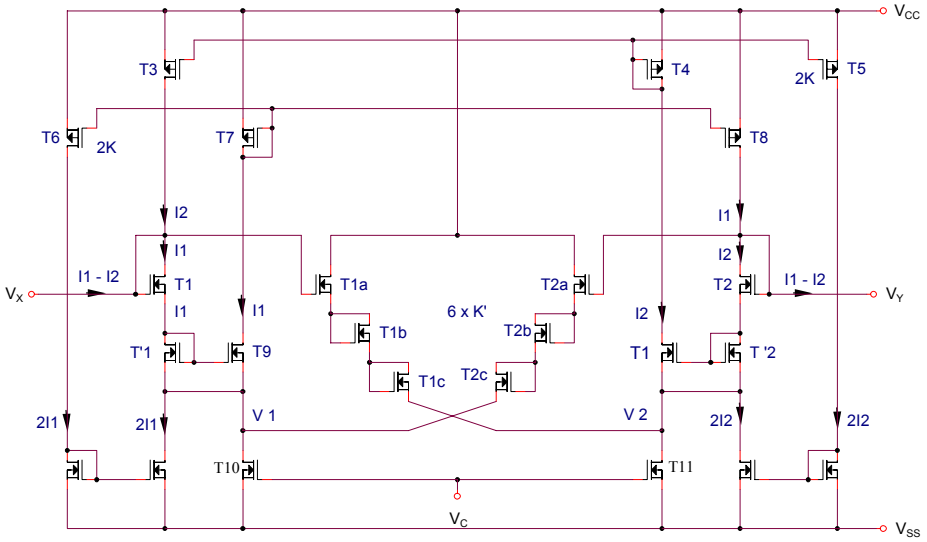

Figure 4: The complete implementation of the CMOS active resistor

2.2. Second-order analysis

The linearity degradation caused the bulk effect was already cancelled using two series combinations of three MOS transistors, T_{1a}, T_{1b}, T_{1c} and T_{2a}, T_{2b}, T_{2c}, respectively. Taking into account the mobility degradation and the channel length modulation, the drain current expression of T_{2a}, T_{2b}, T_{2c} transistors becomes:

$$I = \frac{K'}{2}(V_{GS}'-V_T)^2 \frac{1+\lambda V_{DS}'}{1+\theta_D V_{DS}'} \frac{1}{1+\theta_G(V_{GS}'-V_T)} \quad (4)$$

where θ_D, θ_G and λ are constants from the MOS transistor model. Supposing that the design condition $\theta_D = \lambda$ is fulfilled, the third-order distortion coefficient is:

$$THD_3 = \frac{1}{4}\frac{\theta_G}{V_C - V_{SS}}(V_X - V_Y)^2 \quad (5)$$

The circuit nonlinearity is directly proportional to the square amplitude of the signal applied across the resistor.

3. EXPERIMENTAL RESULTS

The low-power CMOS active resistor was implemented in $0.35\mu m$ CMOS technology and the circuit layout is presented in Figure 5.

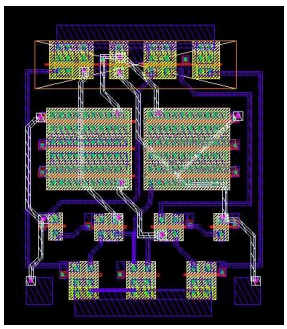

Figure 5: The CMOS active resistor layout

The SPICE simulation $(I_1 - I_2)(V_X - V_Y)$ of the active resistor is presented in Figure 6. In order to estimate the linearity of the circuit, the active resistor is compared with an ideal resistor, resulting the simulated error from Figure 7.

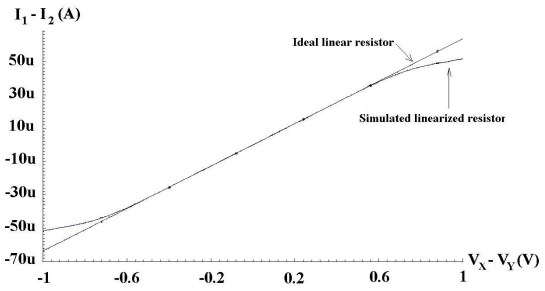

Figure 6: The SPICE simulation $(I_1 - I_2)(V_X - V_Y)$

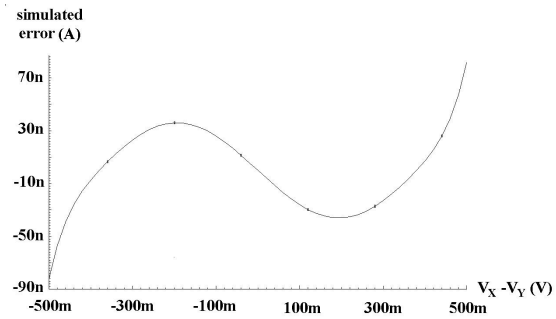

Figure 7: The linearity error

The maximum nonlinearity error of the active resistor for limited input voltage range ($|V_X - V_Y| \le 500mV$) is $error = 0.35\%$.

4. CONCLUSIONS

An original CMOS active resistor with extended input range has been presented. The linearity of the circuit is very good (about 0.35%) for $|V_X - V_Y| \le 500mV$. The circuit operation is not affected by the bulk effect (the equivalent resistance is independent on the threshold voltage). An original design technique allows obtaining a minimizing of the circuit area, $60\mu m \times 80\mu m$. The small value of the circuit supply voltage ($\pm 3.3V$) and the small amount of current consumption allow the utilization of the new proposed active resistor in low-voltage low-power applications. The layout area is minimized using an original technique based on an optimal implementation of the current-controlled voltage generators from the active resistor circuit, being about $60\mu m \times 80\mu m$.

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