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FPGA-BASED EDUCATIONAL LAB PLATFORM

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Abstract: The paper describes a lab platform to study digital design, HDL usage and FPGA implementation. A demo board, the appropriate software tools and an example project are briefly presented.

Key words: FPGA, VHDL, Digital Design, Education.

1 INTRODUCTION

Developing a medium or large digital design is a laborious work. CAD software tools can help in the project description and simulation, while prototype boards are useful to test the design before implementing it in the target technology. On the other hand, learning digital design itself, the CAD tools usage and FPGA basics needs both experimental platforms and educational programs to gradually increase the complexity of projects.

The paper describes a lab platform, composed of a prototype board, the set of lab themes and the design software. Altogether, they can be used either by undergraduate students learning digital design classes and HDL software, or by engineers upgrading their knowledge in the field.

2 THE PROTOTYPE BOARD

DIGILENT SA, a small company in Pullman, Washington State, USA, in close cooperation with the Washington State University department of Electrical Engineering and Computer Science, developed a family of prototype boards, all of them around Xilinx FPGA circuits. Two generations are currently available:

- DIGILAB board, centered on Spartan family of FPGA circuits (XCS05 or XCS10);
- DIGILAB II board, using the Spartan II family representative circuit XC2S200.

Both boards provide, beside the core FPGA device, interface circuits to connect to a PC parallel port (to download the configuring file to the target device), several common input/output circuits/connectors assigned to FPGA pins, and a prototype area. A summary of the provided features follows:

DIGILAB board:

- FPGA supported:- XCS05 (238 logic cells, 5000 logic gates equivalent), or
  - XCS10 (466 logic cells, 10000 logic gates equivalent);
- FPGA socket: - PQ84;
- Supporting (recommended) software:
  - Xilinx Foundation Series V1.5, Student Version;
- Configuring file load sources:
  - PC parallel port (either direct or trough JTAG interface),
  - on board serial ROM socket (stand alone board);
- Digital input circuits (on board):
  - 8 sliding switches,
  - 4 push buttons;
- Digital output circuits (on board):
  - 8 LEDs,
  - 4 digit time-multiplexed seven-segment LED display;
- Standard input/output connectors (on board):
  - RS232 serial port,
  - parallel port (for programming or general purpose),
  - PS2 keyboard connector,
  - VGA connector (1 bit/color only, resistor weighted),
  - stereo audio jack (not connected, to be used in conjunction with prototype area developed circuit),
  - two BNC connectors (not connected, to be used in conjunction with prototype area developed circuit);

DIGILAB II board:

- FPGA: - XC2S200 (5292 logic cells, 200.000 logic gates equivalent);
- Supporting (recommended) software:
  - Xilinx CPLD WebPack ISE;
- Configuring file load sources:
  - PC parallel port (either direct or trough JTAG interface),
  - on board serial ROM socket (stand alone board);

DIGILAB II DIGITAL I/O board (daughter board for DIGILAB II):

- Digital input circuits:
  - 8 sliding switches,
  - 15 push buttons keyboard (2 of 6 encoded);
- Digital output circuits:
  - 16 LEDs,
  - 4 digit time-multiplexed seven-segment LED display;
  - 16 character alphanumeric LCD display;
- Standard input/output connectors:
  - PS2 keyboard connector,
  - VGA connector (2R+3G+3B bit, resistor weighted),

DIGILAB II ANALOG board (daughter board for DIGILAB II – soon available);

3 THE SOFTWARE TOOLS

Xilinx Foundation Series V1.5, Student Version is available on CD-ROM, attached to a series of Digital Design Books edited by Prentice Hall. Each book provides a serial number, which allows obtaining the license file, trough Internet. The license file depends on the Hard Disk serial number, that means is only appropriate to a single target computer. Three license files can be obtained for each software serial number.

The Xilinx supported devices include Spartan FPGA family.

Xilinx CPLD WebPack ISE is free downloadable at the site:
http://www.xilinx.com/xlnx/xil_prodcat_landingpage.jsp?title=ISE+WebPack

The user has to register itself at the same site (free also). The software is modular, each user has to choose the appropriate set of needed modules for the used hardware configuration. Only the simulation module needs a license file, which is free also.

The Xilinx supported devices include Spartan II FPGA family.

Both mentioned software tools provide similar features:

- Design Input File format:
  - Schematic, using standard digital devices library (Xilinx Foundation Series only) or user defined modules (described in one of following formats and used in a hierarchical architecture);
  - State Machine Transition Diagram, for sequential designs;
  - High level Description Languages (VHDL or Verilog).
- Simulation tool to verify the project behavior. The input signals can be simulated:
  - manually, step by step;
  - using a command file to generate the desired test sequence.
- Implementation to the target device. Implementation reports allow analyzing the placing, resource usage degree, time requirements, etc.
- Verification of timing behavior:
  - timing simulation;
  - timing analyzer.
- Programming the device. The software can generate:
  - the file for direct programming the target device. The link can use:
    - parallel cable (direct or using a JTAG adapter);
    - serial cable;
  - the file to be written in the serial PROM. Using this feature, the board can work without a connection to a PC.

4 THE LAB THEMES

A set of lab themes was developed to cover different levels of student knowledge. They start with simple themes, as building (using schematic tools), simulating and implementing simple combinatorial circuits, basic memory devices (NAND and NOR memory cells, D, JK flip-flops, etc.) and grow to complex digital or mixed signal projects (a PC keyboard controlled audio synthesizer, a VGA display controller to generate a game play field, etc).

Figure 2 presents a medium complexity project example: a controller for a two-floor elevator simulator. The student receives an incomplete project containing an input signal DEBOUNCER, a SIMULATOR that uses Digilab's seven-segment displays to simulate elevator behavior (see figure 1) and a DEF_SIM macro to simulate sensor failures. The student must fulfill the project, designing and implementing an elevator controller (ELEV_0M) to "create" an elevator with typical features.

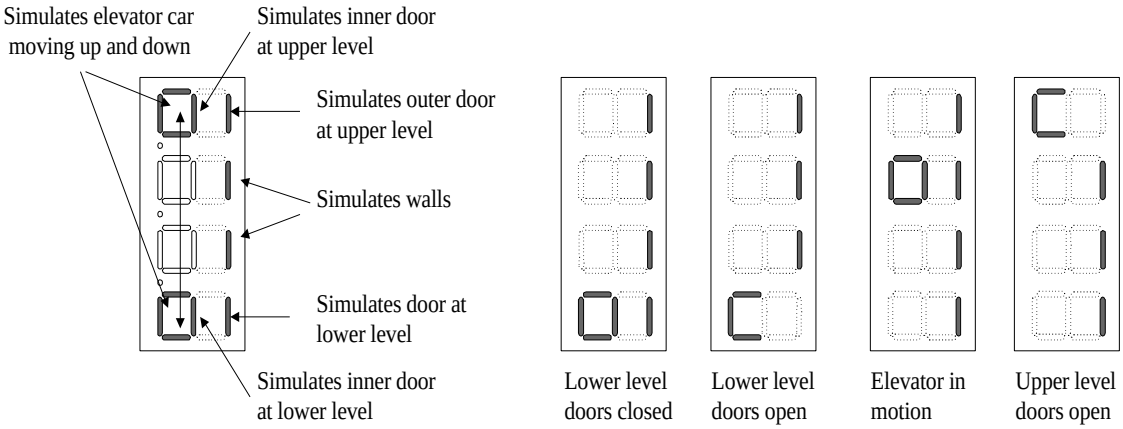
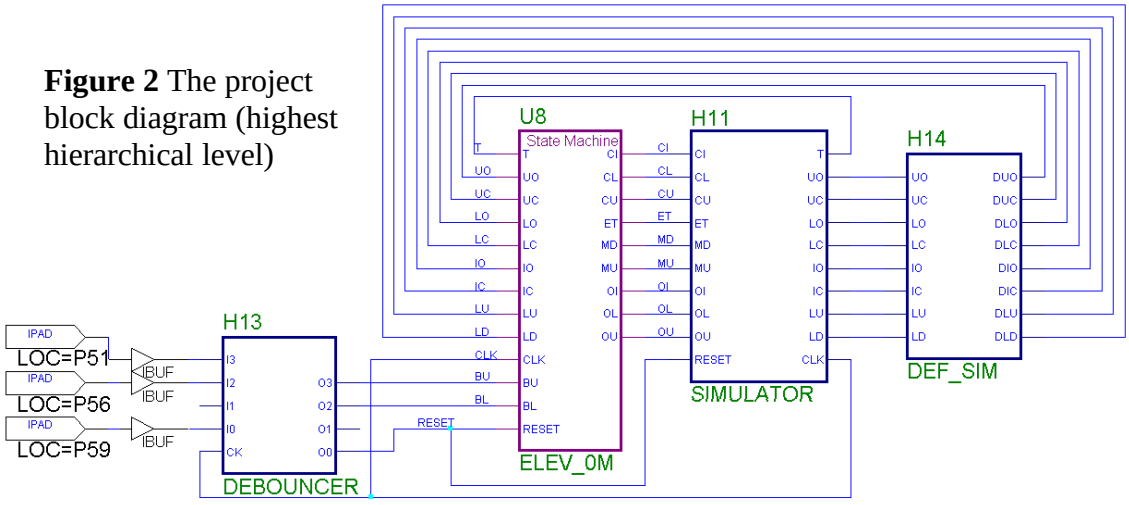


Figure 1 Using the 7-segment display to represent the elevator.

The elevator must respond to a call request at the upper or lower floor by: proceeding to the floor if not already there; opening the doors for a sufficient amount of time; closing the doors, and then waiting for an internal button press. A timer module is provided that to generate sufficient wait times (accessed via the Timer and Enable Timer signals). The timer function should be enabled only when it is required, and left inactive at all other times. The elevator controller requires 10 external inputs (see list below). Two of these inputs model user inputs (push buttons), and eight model sensor inputs. 9 output signals control main and door motors and a timer.

Figure 2 The project block diagram (highest hierarchical level)



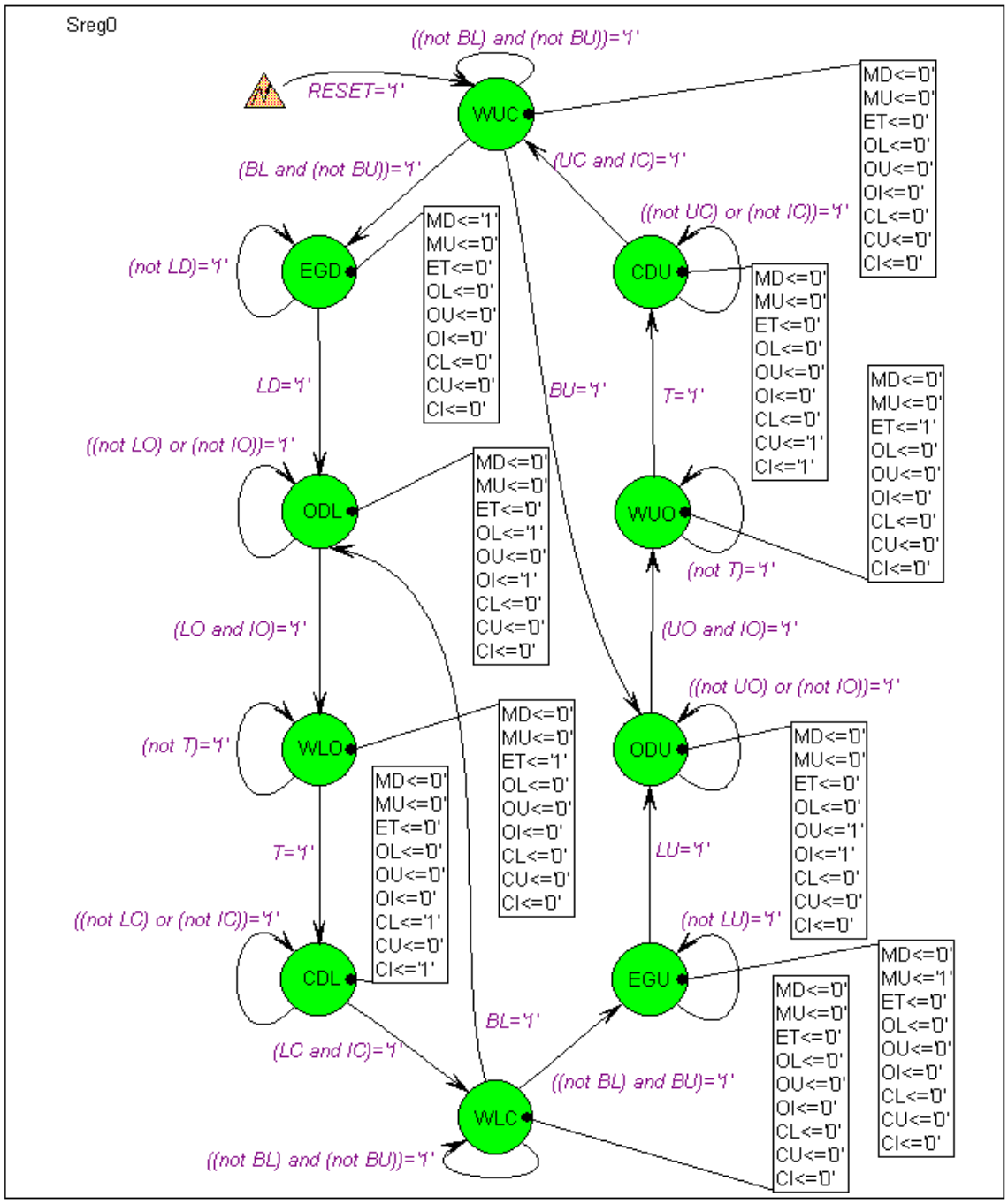


Figure 3 The state diagram edited using the Xilinx Foundation Series State Editor.

The student uses the State Diagram input software feature to generate the ELEV_0M macro, as shown in figure 3. The macro is then used in the block diagram (as shown in figure 2) to replace U8, and the whole project is compiled and downloaded to the target FPGA.

Inputs:

Buttons:

- inner - Go Upper level = GU
  - Go Lower level = GL
- outer - Appeal Upper level = AU
  - Appeal Lower level = AL

Note: instead of signals above, use BU=Button Up and BD=Button Down: BU=GU+AU and BU=GU+AU

Sensors:

- doors
  - external Upper door Open = UO
  - external Lower door Open = LO
  - Inner door Open = IO
  - external Upper door Closed = UC
  - external Lower door Closed = LC
  - Inner door Closed = IC
- level arrived
  - Level Up arrived = LU
  - Level Down arrived = LD
- timer - Timer out = T

States:

Waiting at Upper level Closed doors = WUC
Elevator Going Down = EGD
Opening Doors at Lower level = ODL
Waiting at Lower level Open doors = WLO
Closing Doors at Lower level = CDL
Waiting at Lower level Closed doors = WLC
Elevator Going Up = EGU
Opening Doors at Upper level = ODU
Waiting at Upper level Open doors = WUO
Closing Doors at Upper level = CDU

Outputs:

Main motor: - Go Up = MU
- Go Down = MD

Doors: - Close Upper door = CU
- Close Lower door = CL
- Close Inner door = CI
- Open Upper door = OU
- Open Lower door = OL
- Open Inner door = OI

Timer: - Enable Timer = ET
(timer is continuously reset when ET=0)

5 CONCLUSIONS

The lab platform is used since several years at Washington State University for Digital Design classes (EE214 and EE324) and in Introduction to Microprocessors class (EE314). At Technical University of Cluj-Napoca, the lab platform is used both for an Advanced Digital Design class and as support for graduation works. The co-operation of the two Universities began in 1999-2000 academic year, when Mircea Dabâcan was invited as Visiting Professor at WSU, and consists in developing new lab themes.

The lab boards are sold worldwide by Digilent SA (www.digilent.cc).

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