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LOW COST DATA ACQUISITION

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Abstract: This paper presents a data acquisition interface, designed in educational purpose. It has been designed to be used in some laboratory applications. One of the interface specifications is to implement a cheap, easy to use and acceptable from the viewpoint of performance.

Key words: data acquisition, analog to digital converter, digital to analog converter, serial communication, parallel port.

1. INTRODUCTION

The features of any analogical interfaces are: number of analogical input and output channels, type of ADC and DAC, resolution, max sampling rate, input signal ranges, over voltage protection, configurable inputs: single-ended or differential, FIFO buffer size, data transfers: DMA, interrupts, programmed I/O, relative accuracy, offset error, gain error, input impedance, input bias and offset current, bandwidth, stability. To reduce the complexity of the acquisition board, the interface doesn't contain some modules, drown with dotted line in figure 1. [1]

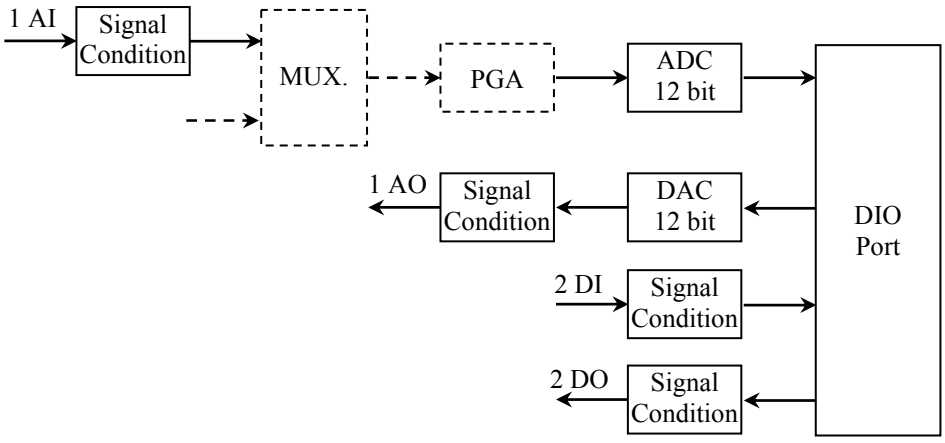

Figure 1

2. HARDWARE

The whole schema is made using two dedicated converters, produced by Linear Technology. The type of communication interface is serial. Because of the reduced number of the lines needed for communication with the two converters, this interface is designed to be used on the parallel port of the computer.

As this interface has been designed to be used on the parallel port of the computer, the decoding logic needed by the intern computer interface has been eliminated. Also the box of the computer doesn't have to be opened for adding an acquisition board. Schematic diagram is shown in figure 2.

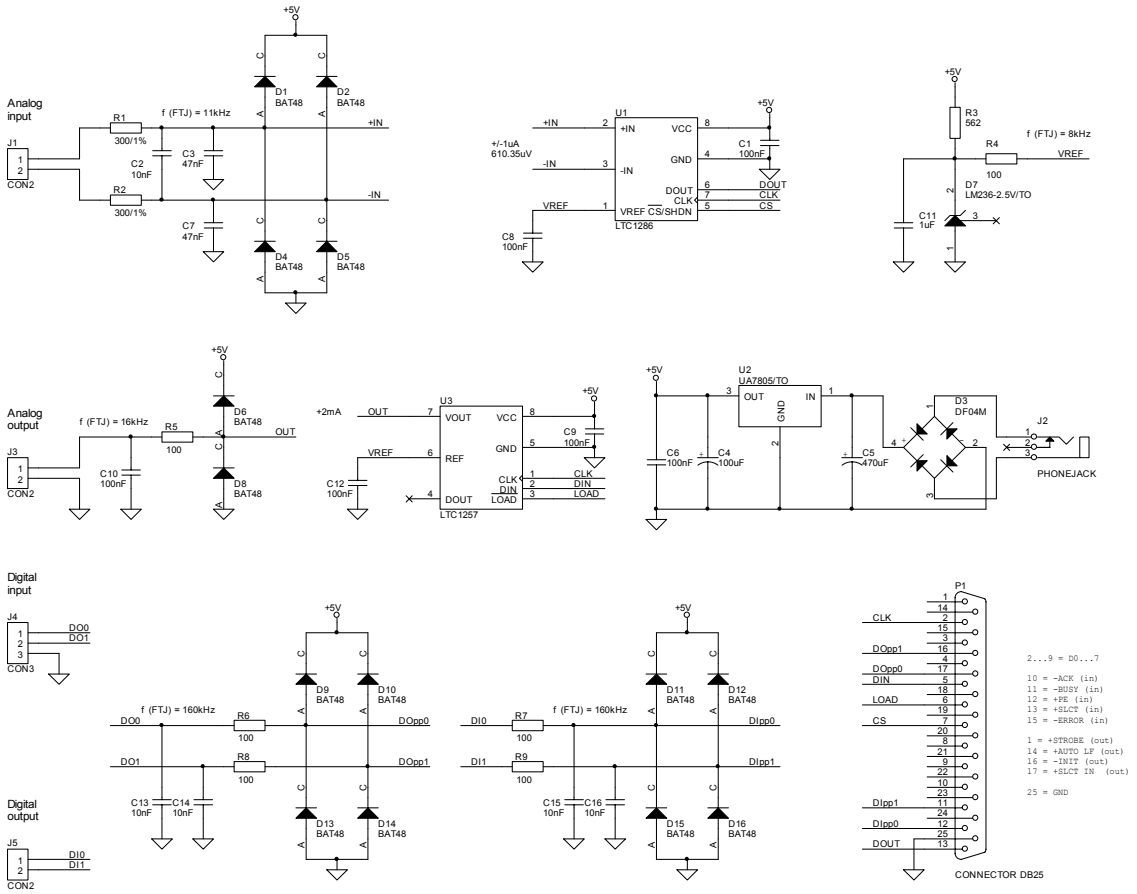

Figure 2

2.1. ADC

LTC1286 are micropower, 12 bit, successive approximation sampling A/D converters. They typically draw only 250 µA of supply current when converting and automatically power down to a typical supply current of 1 nA whenever they are not performing conversions. They are packaged in 8-pin SO packages and operate on 5 V to 9 V supplies. These 12 bit, switched-capacitor, successive approximation ADCs include sample-and-holds. The LTC1286 has a single differential analog input. On-chip serial ports allow efficient data transfer to a wide range of microprocessors and

microcontrollers over three wires. This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers. These circuits can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans (to 1.5 V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages. [2]

2.2. Differential Inputs

With differential inputs, the ADC no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time.

Otherwise, the differencing operation may not be performed accurately. The conversion time is 12 CLK cycles.

Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR(\max)} = V_{PEAK} \cdot 2 \cdot \pi \cdot f("-") \cdot \frac{12}{f_{CLK}}.$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. In most cases V_{ERROR} will not be significant. For a 50 Hz signal on the "–" input to generate a ¼ LSB error (305 μV) with the converter running at CLK = 200 kHz, its peak value would have to be 13.48 mV.

2.3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1286 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

2.4. Reference Inputs for ADC

The LM236-2.5 and LM336-2.5 integrated circuits are precision 2.5 V shunt regulator diodes. These monolithic references operate as low temperature coefficient 2.5 V zeners with a 0.2 Ω dynamic impedance. A third terminal provided on the circuit allows the reference voltage and temperature coefficient to be easily trimmed. The series are useful as precision 2.5 V low-voltage references (V_Z) for digital voltmeters, power supplies, or operational amplifier circuitry. The 2.5 V voltage reference makes it convenient to obtain a stable reference from 5 V logic supplies. Since the series operate as shunt regulators, they can be used as either positive or negative voltage references. LM236-2.5 works for -25°C to 85°C temperature range, while LM336-2.5 works for 0°C to 70°C temperature range. [3]

2.5. RC Input Filtering

It is possible to filter the inputs with an RC network as shown in figure 2. For large values of C (e.g., 0.047 μF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 20pF * V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 64 ms, the input current equals 1.56 mA at $V_{IN} = 5$ V.

In this case, a filter resistor of 300 Ω will cause a voltage drop of 300 μV or ¼ LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time.

2.6. DAC

The LTC1257 is a complete single supply, 12 bit voltage output D/A converter (DAC) in an SO-8 package. The LTC1257 includes an output buffer amplifier, 2.048 V voltage reference and an easy to use three-wire cascadable serial interface. An external reference can be used to override the internal reference and extend the output voltage range to 12 V. The power supply current is a low 350 μA when operating from a 5 V supply, making the LTC1257 ideal for battery-powered applications. The space saving 8-pin SO package and operation with no external components provide the smallest 12 bit D/A system available. [4]

2.7. Parallel Port Interfaces

The LTC1286/LTC1257 can interface directly without external hardware to most popular microprocessor (MPU) synchronous serial formats. If an MPU without a dedicated serial port is used, then 3 or 4 of the MPU's parallel port lines can be programmed to form the serial link to the LTC1286/LTC1257. Normally the CS, CLK and DIN signals would be generated on 3 port lines of the parallel port of computer and the DOUT signal is read on a 4th port line.

2.8. Serial Interface

The data on the DIN input is loaded into the shift register on the rising edge of the clock. The MSB is loaded first and the LSB last. The DAC register loads the data from the shift register when LOAD is pulled low, and remains transparent until LOAD is pulled high and the data is latched.

An internal 5 V regulator provides the supply for the digital logic. By limiting the internal digital signal swings to 5 V, digital noise is reduced. The buffered output of the 12-bit shift register is available on the DOUT pin which will swing from GND to V_{CC}.

Multiple LTC1257's may be daisy chained together by connecting the DOUT pin to the DIN pin of the next chip, while the clock and load signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the LOAD signal is pulled low to update all of them simultaneously. The maximum clocking rate is 1.4 MHz.

2.9. Reference Input for DAC

The LTC1257 includes an internal 2.048 V reference, making 1 LSB equal to 500 μV. The internal reference output is turned off when the pin is forced above the reference voltage, allowing an external reference to be connected to the reference pin. The external reference must be higher than 2.475 V and lower than V_{CC} – 2.7 V, and be capable of driving the 10 kΩ minimum DAC resistor ladder.

If the reference output is driving a large capacitive load, a series resistor must be added to insure stability. For any capacitive load greater than 1mF, a 10Ω series resistor will suffice.

2.10. Voltage Output

The LTC1257 voltage output is able to pull within 2.7 V of V_{CC} while sourcing 2 mA. An internal NMOS transistor with a 200 Ω equivalent impedance pulls the output to ground.

The output is protected against short circuits and is able to drive up to a 500 pF capacitive load without oscillation. If digital noise on the output causes a problem, a simple 100 Ω, 0.1 μF RC circuit can be used to filter the noise.

2.11. PCB Board

The electrical schema and the PCB board have been made using OrCAD. The PCB board of the device has two layers and no vias, so no metallic drills are required for producing it. PCB board is shown in figure 3 and device in figure 4.

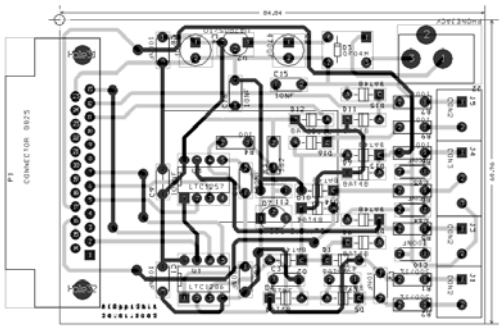

Figure 3

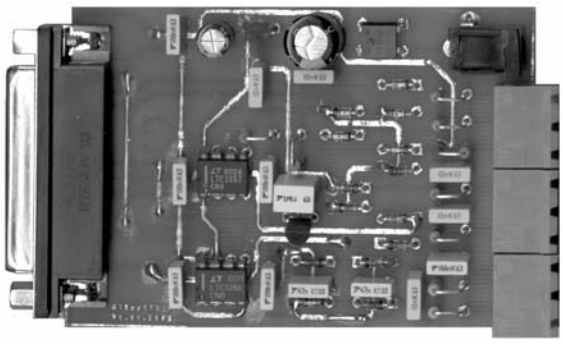

Figure 4

3. SOFTWARE

The interface acquisition driver is implemented in C, so its usage in different programming environment like LabView or Matlab is very easy.

The above example presents an interface implemented in LabView. The linearity of the ADC and DAC converters and the error between the value generated by the DAC and the value read by the ADC, can be easily shown in figure 6. In this example the maximal error is 0.3% on the full scale values.

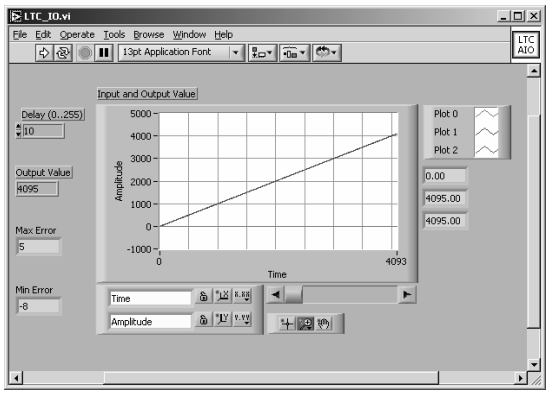

Figure 5

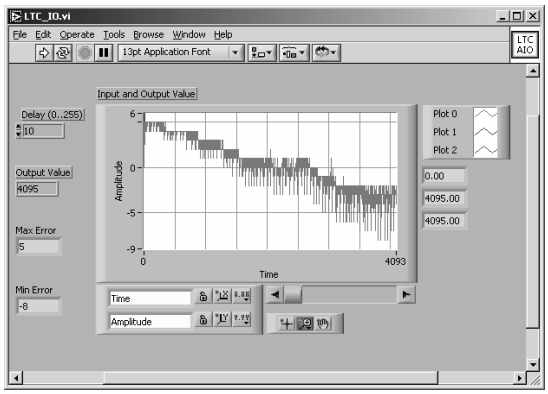

Figure 6

4. CONCLUSION

This system can be easily improved. Because of the reduced power consumption of the circuits, between 100 and 300 mW for 5 V, the circuits can be supplied with power from the signal lines of the parallel port. The power supply of the circuit is implemented in the following way: first, a multi line rectangular signal is generated, and then this signal is rectified and filtered. To implement this, the usage of low-dropout linear regulators, typically 300 mV and some 3 V specified devices is needed. Sometimes the galvanic isolation with optocuplor is more important.

The features of analogical interface are:

- Number of analogical input and output channels: 1,
- Type of ADC: successive approximation,
- Resolution: 12 bit,
- Max sampling rate: 12.5 kS/s,
- Input and output signal ranges: 0V to 2.5V
- Overvoltage protection: ±15V,
- Configurations possibilities: single-ended or differential,
- Data transfers: programmed I/O,
- Relative accuracy: ±3/4 LSB,
- Offset error: ±3/4 LSB,
- Gain error: ±2 LSB,
- Analog Input Leakage Current: ±1μA,
- Output Impedance to GND: 150Ω.

5. REFERENCES

[1] National Instruments, 1996, DAQ Lab-PC-1200/AI User Manual, National Instruments Corporation, June 1996 Edition, Part Number 321230A-01, page A-1;
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[3] Texas Instruments, 1995, LM236-2.5, LM336-2.5, LM336Y-2.5 Integrated Reference Circuits, Texas Instruments Incorporated 1995, SLVS063A.pdf, page 1;
[4] Linear Technology, 1994, Complete Single Supply 12-Bit Voltage Output DAC in SO-8, Linear Technology Corporation 1994, LT1257.pdf, page 1.