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HIGH SPEED VIDEO SIGNAL TRANSMISSION USED IN MULTIMEDIA APPLICATIONS

Laurentiu Gavra(*), Radu Arsinte(**), Dorin Petreus (*), Catalin Constantin(**)
(*)*TedelcoSRL,CaleaTurzii42,Cluj-Napoca,Romania,Email : Laurentiu.Gavra@tedelco.ro*
(*)Technical University Cluj Napoca,str. Baritiu26-28;Email Radu.Arsinte@com.utcluj.ro

Abstract

This paper describes it aspects have met in system design using Panellink concept. This system uses Silicon Image chip set, SIL150 and SIL151, as well as a system built on P87C552 with 8051 core. This whole system is used in automotive information system like a custom passenger information display. The information as well as travelling information, advertising, and a lot of other interesting data can be displayed on LCD flat panel display.

Keywords: Panel link; LCD display; DVI; Multimedia.

1. INTRODUCTION

The SIL 150A PCI-bus transmitter accepts digital parallel data from flat panel graphics controllers and sends it at high speed in encoded serialized form to the receiver. The 150A is capable of receiving data from a 5V flat panel graphics controller if the data is at TTL voltage levels. However, if the output level of the flat panel graphics controller is 5V CMOS level, a voltage divider network is necessary.
The SIL 150 PCI bus transmitter board accepts parallel data from the panel graphics controller, encodes, and serializes this data and sends it to the receiver over three differential data pairs and a differential clock pair. Incoming data can be clocked in at 25- 112MHz., and is transmitted to the receiver at ten times that base 1pixel/clock mode clock rate. Therefore, at an 112MHz 1-pixel/clock mode, data is sent at 1.12Gbits/sec per channel or a total data rate of 3.36Gbits/sec for the entire link.

The SIL 150A is capable of accepting either up 24 bits in 1 pixel/clock mode or up to two 24-bit pixels in 2-pixels/clock mode. Even with this enhanced capability, the panel link cable interconnects physical layer remains unchanged. The SIL150A/151A combination is a single channel SXGA solution and uses the same three data pairs and single clock pairs as previous panel link products. No additional channels or wires are added.

2. PANEL LINK TECHNOLOGY OVERVIEW

The SIL150 and SIL151 are high speed digital interconnect devices for sending video data to digital displays, such as TFT or DSTN Liquid Crystal Displays (LCD). A block diagram of the transmission system is shown in fig 1.

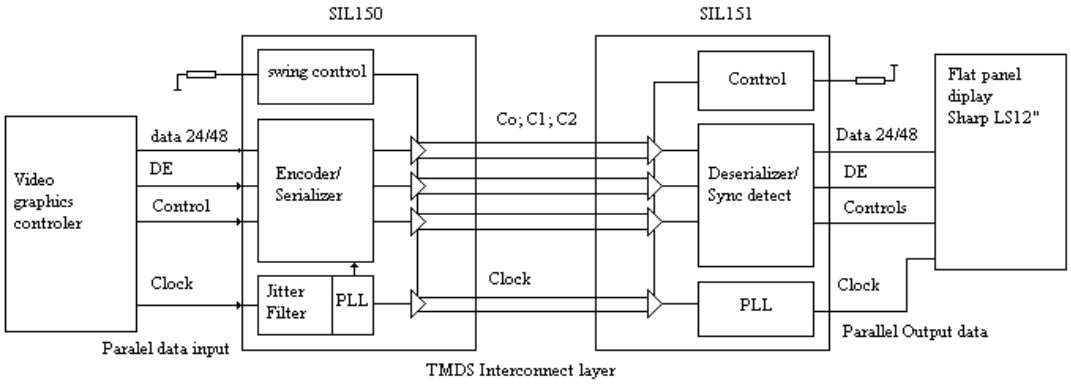

Fig 1. Panel link block diagram

The transmitter receives parallel digital video data from a host graphic controller. Through the use of an internal PLL, the SIL150A encodes and serializes the parallel input data. The serialized data is then transmitted to the Sil151A receiver chip over the Transition Minimized Differential Signaling (TDMS) interconnect layer.

The TMDS interconnect layer consists of three high-speed data channels, C2, C1 and C0 (red, green and blue, respectively) and one low speed clock channel. These signals are sent over four low voltage differential channels, the amplitude of which is set by the swing control circuit of the SIL150. The high-speed data channels have a bandwidth equal to ten times the SiI150 1-pixel/clock frequency, while the differential clock channel has the same
frequency as the 1-pixel/clock frequency. For example, if the input clock is 112MHz at 1-pixel/clock mode or 56MHz at 2-pixels/clock modes, the output channels are 1.12Gbps (Gigabits per second) and the differential clock channel is 112MHz. These signals may be sent over a variety of physical media, such as flex or twisted pair cables. In particular, the encoding of the serial channels is DC balanced, which is required in order for the channels to be capacitive coupled to fiber optic links or systems with independent ground potentials.
The SiI151 receives the serial data and clock from the SiI150. Voltage-controlled resistors internal to the SiI151 terminate the differential signals. The termination control circuit sets the value of resistors. The differential clock is used only as a frequency reference to the internal PLL in the SiI151. The output of this PLL circuit is used to three times over-sample the serial data channels. The over-sampling and encoding enable the data recovery circuits to:

1. Determine the correct sampling point of each data channel individually. That is, the correct sampling point of each high-speed channel is found independently from those of the other two data channels.

2. Determine the frame boundaries on each serial channel individually. The frame boundaries (also referred to as byte boundaries) are the locations within a serial data stream where the data for one byte ends and the data for the next byte begin.

3. Re-synchronize the three data channels to a single PLL generated clock. This resynchronization corrects for inter-channel time skews up to one input clock cycle.

The synchronized data is then decoded back to the original parallel data. The SiI151 provides options to output the data at one 24-bit pixel per clock at the normal clock frequency, or in two 24-bit pixels per clock at half the clock frequency.

The panel link technology uses current mode to electrically drive the cable of the Interconnect Layer. In the following figure Fig2. the cable driving circuit between the transmitter and receiver is shown. Pulling down the cable potential through the pull down devices at the transmitter side develops the signal voltage. The receiver contains the pull-up device, which is a voltage-controlled resistor that provides termination to AVCC. The actual signal voltage will therefore pull down from AVCC (nominally 3.3V) as shown in below.

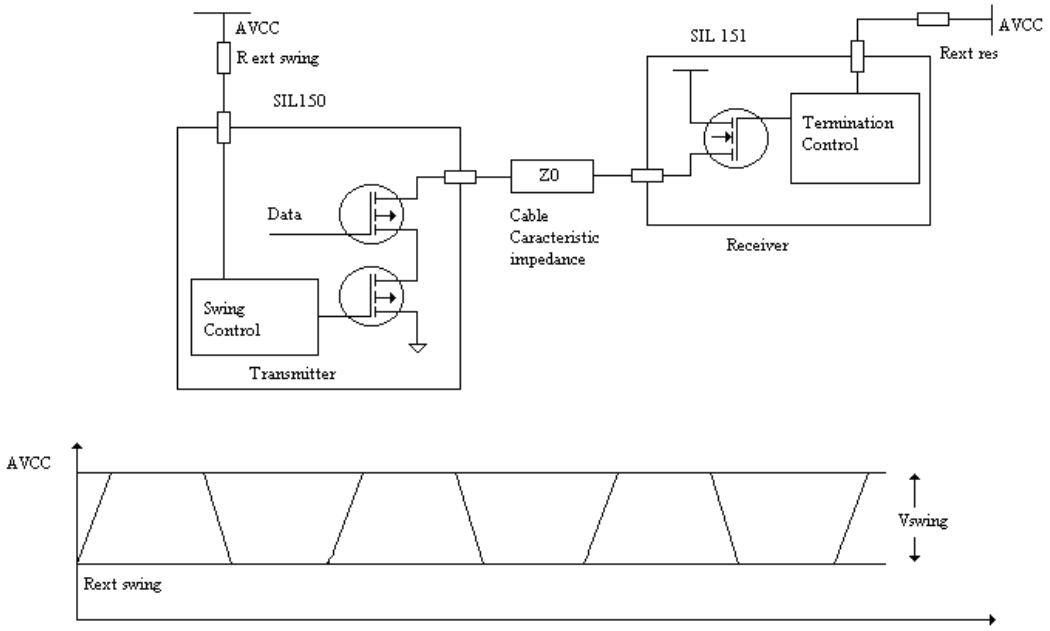

Fig2. Sil 150/151 differential signaling circuit

The amplitude of the differential voltage swing is adjustable through the EXT SWING resistor. The functional relationship between the resistor value and the voltage swing is approximately given by:

$$V_{Swing} = 0.55V * (500ohm / R_{ext\ swing}) \quad (1)$$

Where:

V_{swing} = Single- ended differential voltage swing.
$R_{ext\ swing}$ = Resistor value on EXT_SWING pin.

The larger the voltage swing, the better the signal noise ratio, but the higher the power consumption of the cable driving circuit. The following settings we have used for our application:

$R_{ext\ swing}$ = 510 ohm for 10m cable length and IIC332 kind of cable.

3. CONCLUSION

Pane link Digital technology simplifies PC and display interface design by resolving many of the system level issues associated with high-speed mixed signal design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

Our application implements this technology in automotive information system. It allowed us to connect 8-panel links module in loop through with compact PCI computer. Each panel link is connected with 10m cables from each other and the image is displayed without distortions.

The system was connected in railway street train and the Belgium customer was satisfied with it.

4. REFERENCES

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