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CMOS TRANSCONDUCTOR WITH EXTENDED LINEARITY RANGE

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Abstract: *A CMOS transconductor with an improved linearity range is presented. The expression of the drain current of the MOS transconductor contains odd-order terms, which affect the linearity of the entire circuit. In order to achieve a better linearity by canceling the odd-order distortions, a square-root circuit is used at the output of the differential pair. The analysis of the second-order effects such as the short-channel effect and the mobility degradation shows the necessity of using an additional cross-coupled differential stage to cancel the third-order harmonics.*

Key words: transconductor, linearity, harmonic distortions

1. INTRODUCTION

The transconductor is a basic building block in CMOS analog applications and, because of the quadratic characteristic of the MOS transistor working in saturation, its linearity is rather poor, especially for a large amplitude of the input voltage. As a result, much research has been directed on the design of transconductors with a more linear characteristic. There were used many circuit techniques to improve the CMOS transconductor linearity: a third-order and fifth-order harmonics cancellation [1], [2], a constant-sum of the gate-source voltages circuit connection [3], or a simple linearization of a CMOS transconductor based on square-root circuits [4]. These linearization techniques allow to achieve a constant circuit transconductance only without taking into account the second-order effects such as mobility degradation and short-channel effect, which introduce superior-order terms in the output current versus input voltage expression. This undesired circuit behavior is equivalent with the transconductor linearity degradation, reflected in an increased total harmonic distortions coefficient.

This paper proposes an improved linearity CMOS transconductor, using two square-root modified circuits. Based on the analysis of the performance degradation due to the second-order effects, a third-order cancellation technique will be presented and implemented in 0.35μ CMOS technology. The circuit linearity will be improved by the parallel connection of two quasi-identical transconductors polarized at suitable static

currents. The great advantage of this new circuit comparing with other existing linearity improvement techniques is the possibility of canceling ***the third-order distortion***s (which are the most important) ***due to the second-order effects.***

2. BASIC PROPOSED CMOS TRANSCONDUCTOR

2.1. Analysis of the first-order effects

The CMOS transconductor behavior analysis will be made in a first-order approximation: the drain current of the MOS transistor working in saturation is supposed to be independent on the drain-source voltage and the carriers mobility is supposed to be independent on gate-source and drain-source voltages.

The block diagram of the transconductor is presented in Figure 1. The new proposed idea is to compensate the quadratic characteristic of the MOS transistor by obtaining a current, which is proportional with the square root of the drain current. The difference between these two output currents of the square root circuits will be, theoretically, directly proportional with the differential input voltage.

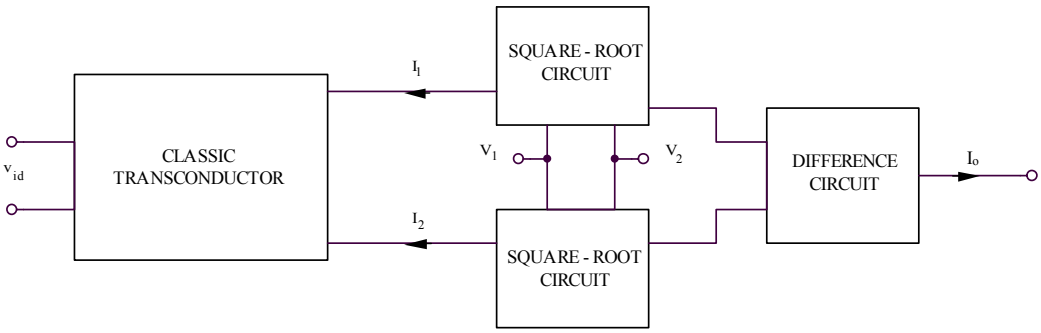

Figure 1: The block diagram of the transconductor

The CMOS implementation of the block diagram from Figure 1 is presented in Figure 2.

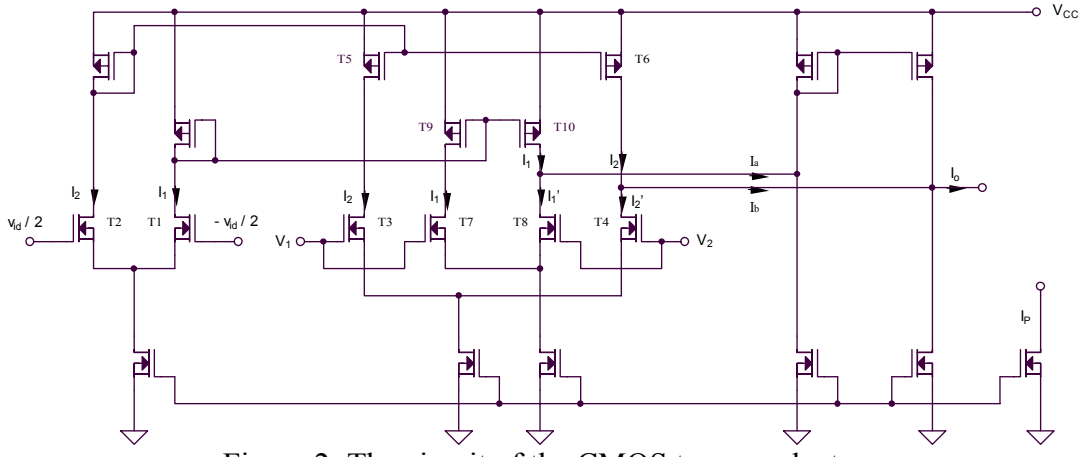

Figure 2: The circuit of the CMOS transconductor

Q_1 and Q_2 transistors form the transconductor core with the output currents I_1 and I_2 having the following expressions:

$$I_{1,2} = \frac{K_0}{2}\left(V_{GS_{1,2}} - V_T\right)^2 = \frac{I_P}{2} \pm \frac{I_P}{2}\left(\frac{K_0 v_{id}^2}{I_P} - \frac{K_0^2 v_{id}^4}{4I_P^2}\right)^{1/2} \quad (1)$$

Taking only the first four terms from theirs expansions, the drain currents expressions can be written as follows:

$$I_{1,2}(v_{id}) = \frac{I_P}{2} \pm \frac{K_0^{1/2} I_P^{1/2}}{2} v_{id} \mp \frac{K_0^{3/2}}{16 I_P^{1/2}} v_{id}^3 \mp \frac{K_0^{5/2}}{256 I_P^{3/2}} v_{id}^5 \quad (2)$$

So, because odd-order nonlinearities will apear without designing a linearisation technique, two square root circuits, consisting in $Q_3 - Q_6$ and $Q_7 - Q_{10}$ transistors are introduced to improve the circuit linearity. Considering that all transistors are working in saturation, the output currents of the square root circuits are:

$$I_{a,b} = I_{1,2} - I'_{1,2} = -\frac{K_0}{2}(V_1 - V_2)^2 + \sqrt{2K_0}(V_1 - V_2)\sqrt{I_{1,2}} \quad (3)$$

The output current of the entire CMOS transconductor will be:

$$I_o = I_b - I_a = \sqrt{2K_0}(V_1 - V_2)\left(\sqrt{I_2} - \sqrt{I_1}\right) \quad (4)$$

Because of the operation of MOS transistor in the saturation region, the differential input voltage v_{id} depends on the square root of the drain current difference:

$$v_{id} = \sqrt{\frac{2}{K_0}}\left(\sqrt{I_2} - \sqrt{I_1}\right) \quad (5)$$

resulting the transconductor output current expression:

$$I_o = K_0(V_1 - V_2)v_{id} \quad (6)$$

In conclusion, the theoretical analysis made by neglecting the second-order effects shows an absolute linearity of the transconductor from Figure 2.

2.2. Analysis of the second-order effects

The expression (1) of the drain currents is written by neglecting the second-order effects such as the short-channel effect and the mobility degradation, which are modelled by the following relation:

$$I_{1,2} = \frac{K_0}{2}(V_{GS_{1,2}} - V_{T_{1,2}})^2 \frac{1 + \lambda V_{DS_{1,2}}}{[1 + \theta_G(V_{GS_{1,2}} - V_{T_{1,2}})](1 + \theta_D V_{DS_{1,2}})} \quad (7)$$

where θ_G, θ_D are process constants and λ models the Early effects. For this real case, considering the design condition that $\theta_D = \lambda$ and supposing that Q_1 and Q_2 transistors are identical, that is $V_{T_1} = V_{T_2} = V_T$, the differential input voltage expression is:

$$v_{id} = \sqrt{\frac{2}{K_0}}\left[\left(\sqrt{I_2} - \sqrt{I_1}\right) + \frac{\theta_G^2}{4K_0}\left[(I_2)^{3/2} - (I_1)^{3/2}\right]\right] \quad (8)$$

and the output currents of the square root circuits are:

$$I_{a,b} = I_{1,2} - I'_{1,2} = -\frac{\theta_G^2}{2K_0} I_{1,2}^2 - \frac{K_0}{2}(V_1 - V_2)^2 + \sqrt{2K_0}(V_1 - V_2)\sqrt{I_{1,2}}\left(1 + \frac{\theta_G^2}{4K_0} I_{1,2}\right) \quad (9)$$

The output current of the transconductor has the following quasi-exactly expression:

$$I_o = \frac{\theta_G^2}{2K_0}\left[(I_1)^2 - (I_2)^2\right] + \sqrt{2K_0}(V_1 - V_2)\left[\left(\sqrt{I_2} - \sqrt{I_1}\right) + \frac{\theta_G^2}{4K_0}\left[(I_2)^{3/2} - (I_1)^{3/2}\right]\right] \quad (10)$$

Using (8) and (10) relations, the transconductor output current will be given by:

$$I_o = K_0 v_{id}(V_1 - V_2) + \frac{\theta_G^2}{2K_0}\left[(I_1)^2 - (I_2)^2\right] \quad (11)$$

where the first term is the desired linear term and the second one is the error introduced by the second-order effects. Using relation (5) of the differential input voltage, it results the polynomial expansion of the transconductor output current:

$$I_o = \frac{\theta_G^2 I_P}{2}\sqrt{\frac{I_P}{K_0}}\left(v_{id} - \frac{K_0}{8I_P} v_{id}^3 - \ldots\right) + K_0(V_1 - V_2)v_{id} \quad (12)$$

The approximate expression of the third-order distortion coefficient is:

$$THD_3 = \frac{\theta_G^2 v_{id}^2}{16(V_1 - V_2)}\sqrt{\frac{I_P}{K_0}} \quad (13)$$

3. THE IMPROVED CMOS TRANSCONDUCTOR WITH THIRD-ORDER DISTORTIONS CANCELLATION

In order to cancel the main cause of nonlinearity represented by third-order distortion, two identical circuits are connected in Figure 3 with the input pins interchanged.

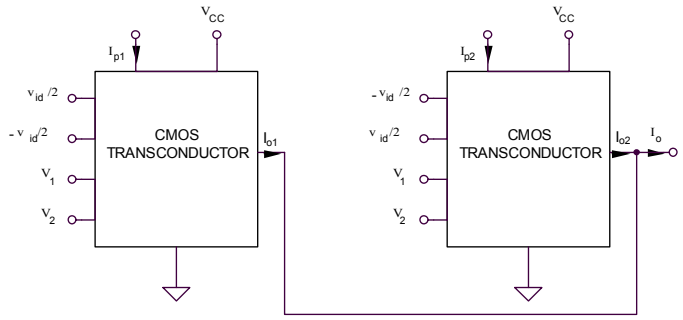

Figure 3: CMOS transconductor with third-order distortion cancellation

So, considering that the polarization current I_P is different for the two transconductor (otherwise, the output current of all the circuit from Figure 3 will be zero because I_o is an odd function on v_{id}), it results the expressions of I_{o_1} and I_{o_2}:

$$I_{o_{1,2}} = \frac{\theta_G^2 I_{P_{1,2}}}{2}\sqrt{\frac{I_{P_{1,2}}}{K_{0_{1,2}}}}\left(v_{id} - \frac{K_{0_{1,2}}}{8I_{P_{1,2}}}v_{id}^3 - \frac{K_{0_{1,2}}^2}{64I_{P_{1,2}}^2}v_{id}^5\right) + K_{0_{1,2}}(V_1 - V_2)v_{id} \quad (14)$$

So, the condition of canceling the third-order distortions is $I_{P_1}K_{0_1} = I_{P_2}K_{0_2}$, resulting the expression of the output current of the transconductor from Figure 3:

$$I_o = I_{o_1} + I_{o_2} = \frac{\theta_G^2}{2}\frac{I_{P_1}^2 - I_{P_2}^2}{\sqrt{K_{0_1}I_{P_1}}}v_{id} + \frac{\theta_G^2}{128}\frac{K_{0_2}^2 - K_{0_1}^2}{\sqrt{K_{0_1}I_{P_1}}}v_{id}^5 + (K_{0_1} - K_{0_2})(V_1 - V_2)v_{id} \quad (15)$$

Now, mainly because of the fifth-order harmonic, the distortion coefficient is decreasing to:

$$THD_5 = \frac{\theta_G^2}{128}\frac{K_{0_1} + K_{0_2}}{\sqrt{K_{0_1}I_{P_1}}}\frac{1}{V_1 - V_2}v_{id}^4 \quad (16)$$

4. EXPERIMENTAL RESULTS

The circuit was implemented in 0.35μ CMOS technology. The SPICE simulation output current vs. differential input voltage is presented in Figure 4.

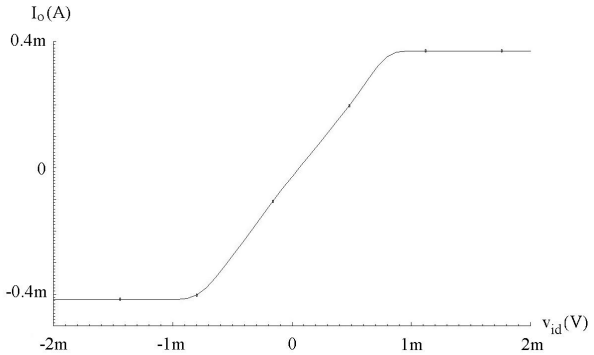

Figure 4: SPICE simulation of $I_o = I_o(v_{id})$

So, a very good linearity of the transconductor is achieved. The small value of the circuit supply voltage ($3.3V$) and the very small current consumption make it compatible with low-power low-voltage applications.

The layout of the CMOS transconductor, realized in 0.35μ CMOS technology is presented in Figure 5. The approximate silicon occupied area is about $40\times 45\mu m$.

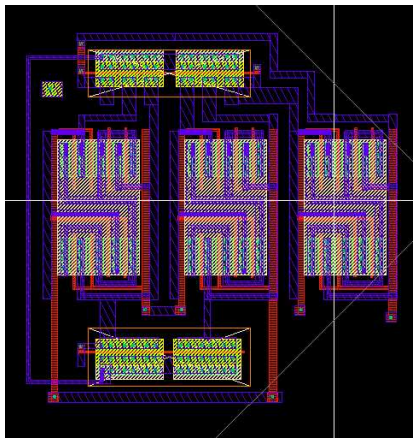

Figure 5: CMOS transconductor layout

5. CONCLUSIONS

It was presented a linearisation technique for a CMOS transconductor. In order to extend the linearity range, two square-root circuits were used to compensate the quadratic characteristic of the MOS transistor working in saturation. The harmonic distortions introduced by the second-order effects were reduced using an additional quasi-identical transconductor excited with an opposite input voltage. With a small supply voltage and current consumption, the proposed CMOS transconductor could be used, for example, in medical applications.

6. REFERENCES

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