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TOPOLOGICAL DETERMINATION OF THE EQUIVALENT NETWORK FOR RECIPROCAL AND SYMMETRICAL MULTIPOL CIRCUITS

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Abstract. The paper presents an original method for topological determination of network function for linear, symmetrical and reciprocal multipols interconnected in networks with a great number of nodes and branches. The algorithm used has five stages: the initial description of each multipol, the description of the interconnected multipol topology, the interconnection vector generation, the reducing of blocks and networks obtained by their successive interconnection and finally the topological determination of network function for couples of ports of an interconnected multipol system. Thus, the original algorithm using interconnection associated vectors, presented in this paper, simplifies and orders the eliminating methods determination of the equivalent multipol.

Key words: topological, symmetrical, reciprocal, multipol, equivalent.

1. INTRODUCTION

The method proposed in this paper is a very efficient and original one permitting not only a topological description of the multipol network and multipol parameters but also a simplified description of the multipol interconnection and an ordered algorithm of access poles, an elimination algorithm of internal nodes, an evaluation algorithm of multipol interconnection included generation of a currently set of interconnection nodes and finally the determination of transfer function from a port α to a port β of a interconnected multipol system [1]. The application of the proposal method allows a direct topological determination of the network functions referring to the given access ports [2].

2. TOPOLOGICAL DESCRIPTION OF MULTIPOL ELEMENTS

For topological description of multipol parameters, each linear and reciprocal element component of multipol is to be characterised using complex admittance or operational admittance,Y. Using equivalent edges that replace serial or parallel elements, are to be considered multipols without serial or parallel elements.

For generalisation (having in view the generation of the complex polygon structure by the complete star-polygon transformation) we shall further take into consideration the complete polygon structure of the multipol. For each linear, symmetrical and reciprocal

multipol there will be a triangular tableau model to associate with a fictitious complete polygon circuit of identical vertex.

The contained elements of this tableau will be the ordered admittance of the multipol edges and "zeros" for the "non-existent" edges of characteristic structure. A circuit complete pentagon (N = 5) is shown in fig.1.

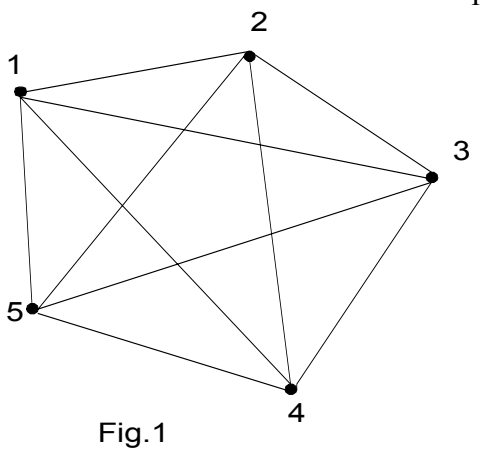

Fig.1

Network graph with complete pentagon

	2	3	4	5
1	Y_{12}	Y_{13}	Y_{14}	Y_{15}
2		Y_{23}	Y_{24}	Y_{25}
3			Y_{34}	Y_{35}
4				Y_{45}

Fig.2.
Admittance associated triangular tableau

The edges parameters are disposed in the associated triangular tableau (fig.2) which has N-1 lines (1, 2,..., N-1) and N-1 columns (2, 3,..., N). The triangular tableau is associated with parameter vector V which has N(N-1)/2 elements.

3. THE ALGORITHM METHOD FOR MULTIPOLS REDUCTION

The vertices of the interconnected multipol network, derived from the overlapping of at least two vertices pertaining to different multipols, are refereed to as network link vertices. The types of vertices given below define the vertices of the interconnected multipol network. The *primary vertices* (input vertices) of an interconnected multipol network are, by definition, network vertices that can be either access vertices or link vertices. The *secondary vertices* (internal vertices) of the interconnected multipol network are, by definition, multipol vertices that are not primary vertices. Each network multipol is associated to a multipol primary vertex vector which are, by definition, multipol vertices and at the same time network primary vertices. We consider a succession of multipols 1, 2,..., NB where each new input multipols marks an interconnected multipol. Each block may be reduced (as vertices number) by eliminating the block vertices which are secondary blocks in the interconnected block network. This reduction is achieved by successive star-polygon complete transfiguration which eliminates one of the secondary vertices at a time. Each common BC_K block where k = 2, 3, …, NB -1 gets simplified by the replacement of the derivation elements pairs with an equivalent element and by successive star-polygon transfiguration which remove the block vertices to be eliminated from the each common block are the overlapped primary vertices that are not external access vertices and to which no primary vertices of the following blocks k+1, k+2, …k+ NB -1 are to be connected. This elimination can be done by the same star-polygon complete transfiguration which eliminates the neutral point of the star. Thus, the simplification of the BC, common block can be achieved through successive star- complete polygon transfiguration which reduces the block vertices that are to be eliminated according

to vertices numbering. After each transfiguration, the derivation edges are reduced getting replaced by an equivalent edge. For the star-complete polygon transfiguration applied to one vertex of an electric linear reciprocal circuit, represented by the associated triangular tableau one might find an extremely efficient algorithm suggested here bellow.

We shall consider, as an example NA external access vertices which can be reduced to a complete polygon network having NA vertices. For the elimination of the supplementary access vertices reducing the greatest order number will be selected. For instance, having NA= 3 external access vertices (1,5 input and 4,5 output, where the 5 node can be electroenergetical system null [4] or common base in electronic circuits) the number order will be : N -3, N -2, N -1, N which can be seen in fig. 3,a (for N = 5).

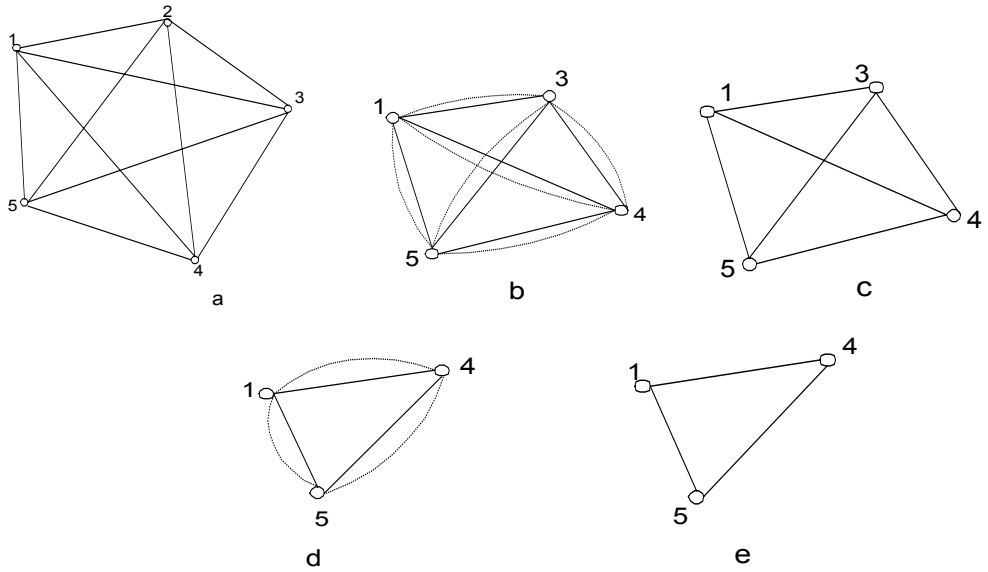

Fig.3- Network graph with complete pentagon and the access vertices 1, 4, 5: elimination of the stars with the centre in the vertex 2 (a-b) and the vertex 3(c-d). Tripol equivalent network (e).

The equivalent network can be obtained through N-NA complete star polygon successive transfiguration. The vertices 1, 2,…, N-NA being successively eliminated. The elimination of vertex 2 (from the N vertices polygon) for obtaining the edge for the equivalent polygon in relation with the vertices 2, 3,.., N, requires:

a) The edge admittance calculation of the complete polygon, equivalent with the star network having the centre in the vertex 2 and the vertices 2, 3,…, N;

b) Replacing the edge pairs, in parallel connection with each vertex pair, with an equivalent edge. The successive vertex elimination, from the vertex 2 to the vertex N- NA is made by recurrence with the relation:

$$Y_{e,h_j}^{(i-1)} = \frac{y_{lh}^{(i-1)}}{\sum_{l+1}^{N} Y_{l_q}^{(i-1)}} \qquad (1)$$

where the upper index corresponds to the eliminated vertex and the index e is used for the polygon equivalent with the star network, associated with the eliminated vertices. For generality, $Y_{kj}^{(0)} = Y_{kj}$ corresponds to the admittance from the initial complete polygon.

For the considered network having the centre in vertex 2 (fig.3, b and 3, c) and respectively the star network having the centre vertex 3 (fig. 3, d and 3, e). The complete equivalent polygon with 3 vertex access (1, 5 and 4, 5) is a classical Π- scheme, and is represented in fig.3, e. The admittance triangular tableau corresponding of this network is represented in figure 4.

	4	5
1	$Y_{14}^{(2)}$	$Y_{15}^{(2)}$
4	-	$Y_{45}^{(2)}$

Fig.4- Admittance triangular tableau for the network having the graph from figure 3, e.

For the considered order the elimination is done efficiently in the order 1, 2,.., NVI (internal vertices number) or (1, 2,.., N-NA). After the first i-1 elimination have been done, the triangle resulting from the elimination of the first i-1rows, has to be processed. Consequently, the following algorithm can be applied with the stages 1= 1, 2,..., NVI. For the stages corresponding to vertex i:

1. Calculate the sum S_i of the admittance situated on the row i and liked to the vertex N:

$$S_i = \sum_{k=i+1}^{N} Y_{i,k}^{(i-1)} \tag{2}$$

where $Y_{i,k}^{(i-1)}$ is the admittance of the edge which links the vertex i to vertex h ≥ i after the first i-1 internal vertices have been eliminated;

2. Calculate the rapport: $\alpha_{i,k} = \frac{Y_{i,k}^{(i-1)}}{S_i}$; k = i+1, i+2, ...N-1 (3)

which values are memorised into the vector VM.

3. For each row with j < i the elements of the line are replaced by:

$$Y_{j,k}^{(i)} = Y_{j,k}^{(i-1)} + Y_{i,j}^{(i-1)} \alpha_{i,k} \tag{4}$$

Thus, this triangular model simplifies and reduces the elimination of the vertex permitting the gradual reducing of calculation area. By interconnecting the first "k" blocks, one obtains the common multipol BC_k containing:

- reducible nodes and
- irreducible nodes (external access nodes and interconnection nodes with the next k+1, k+2,..., NE nodes).

The successive transfiguration algorithm presented here bellows is used for reducing of reducible nodes. Each interconnection of the BC_K block with the preceding BC_{K-1} block involves an overlapping of nodes leading to a shunt connection of some circuit elements. As consequence, the block system reduction involves the reduction of the shunt elements too. This represents a necessary condition for proposed successive transfiguration algorithm application.

5. EXAMPLE

Let's consider a complete and symmetrical polygon central circuit with n vertices and n = NB complete and symmetrical peripherals polygon (n blocks) with m vertices each connected to two coupling vertices to every of the external edge of the central polygon. In figure 5 we can see an example in which n = 6 and m = 5. Each edge has admittance Y=2 S.

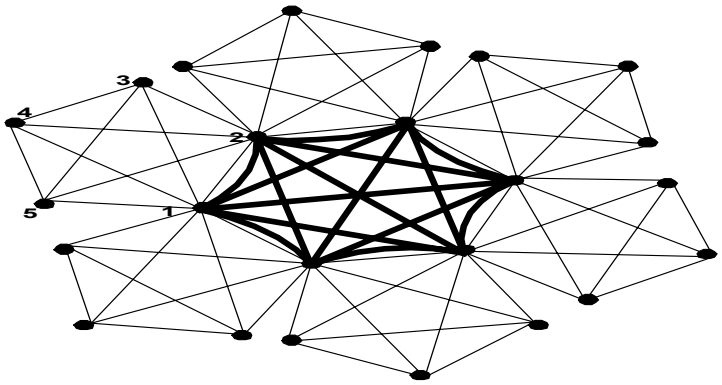

Fig. 5- The interconnected multipol having a central complete hexagon and 6 complete peripherical complete pentagon connected to 2 coupling vertices with central polygon.

The system of interconnected multipol has 24 vertices and 75 edges. The system has NA = 4 external access vertices: the input port α with 1, 2 input vertices, and the output port β with 9, 16 output vertices. Each (NB = 6) peripheral block may be reduced (as vertices number) by eliminating the block vertices which are secondary blocks in the interconnected block network. For example, the reduction of the peripheral block which has 1, 2, 3, 3, 4 and 5 vertices, fig.6, a, is successive done only through star-complete polygon transfiguration keeping 1 and 2 coupling and access vertices. The elimination of the vertices 4, 5, shown in figure 6, b and c, and on vertices number 3 - which is practically includes in the series of the coupling vertices 1, 2- is described in figure 6, d. Thus we obtain the equivalent cuadripol which has 1, 2, 9 and 16 vertices.

The appeal of the computation procedure of the network functions from the port α (1, 2) to the port β (9, 16), relations (10) and (12), offers the results: $Y_{\beta\alpha} = Y_{(9, 16), (1, 2)} = 0$, 95 S.

The TURBOPASCAL programmes established on the basis of this method for the microcomputer PENTIUM IV computes this complete circuit in 45'', [5].

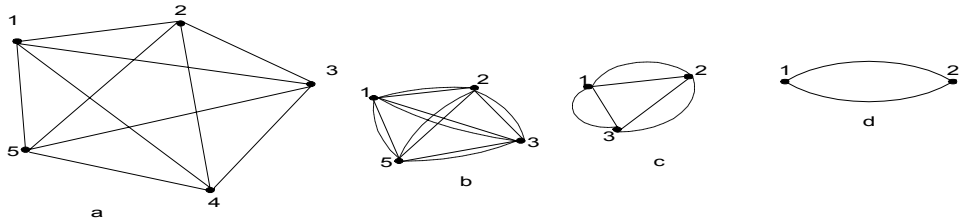

Fig.6-The reduced of one (a) of the periphricals complete pentagon by eliminating the secondary vertices: 4 (b), 3 (d).

6. CONCLUSIONS

Equivalent network determination for diverse electroenergetic and electronic multipol systems represents an extremely important problem in the context of trying an adequate iterative method permitting efficient and fast calculation.

The proposed method is an original algorithm which eliminates the sign factor problem for the network function calculation, simplifies and orders the eliminating methods determination of the equivalent multipol.

The method is highly useful and efficient for great complexity electrical network analysis.

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